422 and 485 Standards Overview and System Configurations

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ABSTRACT

ANSI TIA/EIA-422 and TIA/EIA-485 standards, commonly known as 422 and 485, respectively, specify balanced data-transmission schemes for transmitting data over long distances in noisy environments. These standards are compared, and their basic differences and similarities are discussed. Techniques for impedance matching to minimize line reflections in several applications are presented, with laboratory test results.

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Introduction

The 422 and 485 standards, as they are known today, are balanced data-transmission schemes that offer robust solutions for transmitting data over long distances and noisy environments. The official titles for these two standards are ANSI TIA/EIA-422 and TIA/EIA-485, respectively, and are revised periodically by the TR-30.2 DTE-DCE Interfaces and Protocols Subcommittee to the Telecommunications Industry Association (TIA) TR-30 Data Transmission Systems and Equipment Committee. The RS prefix, which has been used for many years on both standards, is no longer in use. Generally, it is thought that this prefix means Recommended Standard, but actually it means Radio Sector. For identification, 422 and 485 suffice.

This application report offers an overview of the 422 and 485 standards. While many specifications are described in the official ANSI documents, only the most prevalent are discussed in this application report. The purpose of this application report is to not duplicate the official documents, but to outline basic differences and similarities between the 422 and 485 standards. Major specifications are described in detail and the two standards are compared. Because impedance matching is an important aspect of differential data transmission in minimizing line reflections due to transmission-line effects, techniques for terminating different system applications are presented. Also, typical system configurations are taken into consideration for optimal application performance and cost constraints.

Overview of 422 and 485 Standards

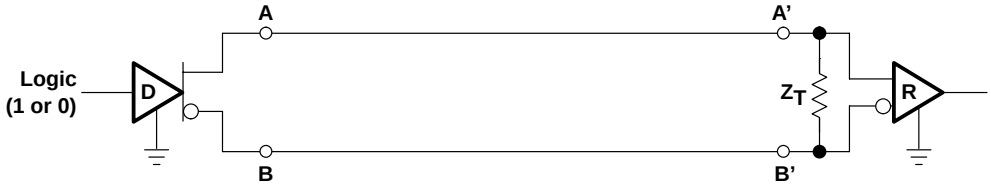
Officially, the 422 standard's title is *Electrical Characteristics of Balanced Voltage Digital Interface Circuits*, and is published by the ANSI Telecommunication Industry Association/Electronic Industries Association (TIA/EIA). In the industry, the term 422 is commonly used rather than the official name, and this document does the same. 422 is specified as a simplex multidrop standard, which means only one driver and up to ten receivers can be attached to a bus.

The 485 standard's title is *Electrical Characteristics of Generators and Receivers for Use in Balanced Digital Multipoint Systems*. 485 is commonly used, rather than its official title. If more than one driver is required, devices conforming to 485 are recommended. 485 specifications allow only one driver to send data at a time, and up to 32 unit loads (U.L.) can be placed on the bus. The U.L. concept is described in this application report in the *Selected 485 Electrical Specifications* section.

422 and 485 initially might appear to be similar, but are distinct, and interchangeability is determined by the bus architecture. The 485 standard is written to be electrically compatible with 422. To illustrate their basic differences, a condensed description of each standard is presented in the following subsections.

Selected 422 Electrical Specifications

The balanced-voltage digital interface is shown in Figure 1. The driver (or generator) is labeled D, the receiver is labeled R, and the termination impedance is Z_T. The termination impedance should be equal to the characteristic impedance of the cable, Z_0, and is used only once at the end of the cable. Because matching termination impedance to Z_0 often is difficult to achieve and is application dependent, typically, ±20% is sufficient. Also, up to nine additional receivers can be placed along the cable from points A and B to points A' and B', respectively. No restriction on maximum cable length is imposed by the 422 standard. Taking this into account, systems of up to 1 km are not uncommon, with signaling rates no higher than about 100 kbps. Speed and cable lengths work against each other. In other words, the longer the cable, the slower the signaling rate must be, while data can be transmitted faster on shorter cables. As a rule of thumb, the data signaling rate (in bps) multiplied by the cable length (in meters) should not exceed 10^8. For example, a system with a cable measuring 500 m should not transmit data at speeds greater than 200 kbps (10^8/500).



NOTES: A. D = driver (or generator)
B. R = receiver
C. Z_T = termination impedance

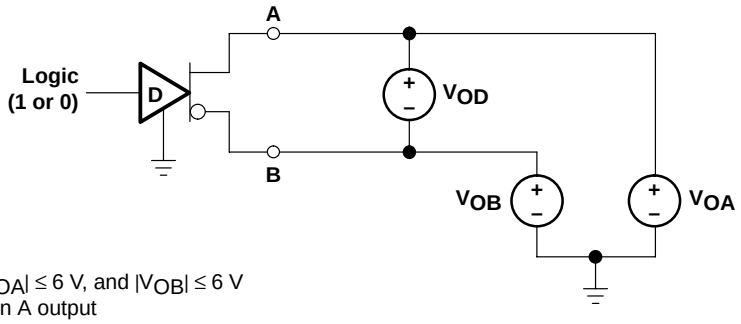
Figure 1. Balanced-Voltage Digital-Interface Circuit

Although the input electrical characteristics of the 422-compliant receiver are identical to those of the 423-compliant receiver (ANSI TIA/EIA-423 standard), the 423 specifies an unbalanced signaling scheme, which is not within the scope of this application report.

Descriptions of selected specified parameters are presented in the following paragraphs.

Open-Circuit Output Voltage (V_{OD}, V_{OA}, and V_{OB} Measured)

The output voltage shall not exceed ±6 V under unloaded conditions, and the differential voltage [measured as the difference between an output voltage, V_{OA} (V_{OB}), and its complementary output voltage, V_{OB} (V_{OA})] is no greater than ±10 V. See Figure 2 for the test circuit.

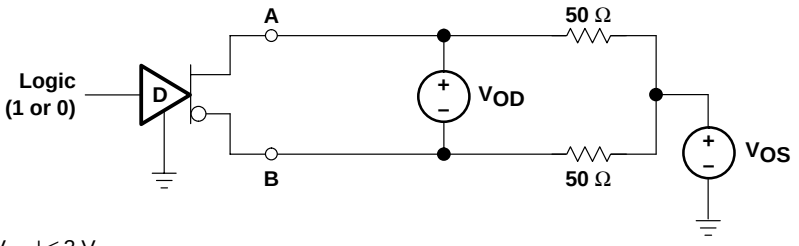


NOTES: A. $|V_{OD}| \le 10$ V, $|V_{OA}| \le 6$ V, and $|V_{OB}| \le 6$ V
B. V_{OA} = voltage on A output
C. V_{OB} = voltage on B output
D. V_{OD} = differential output voltage

Figure 2. Open-Circuit Test Circuit

Differential and Offset Output Voltage (V_{OD} and V_{OS} Measured)

To ensure proper drive strength, a minimum of ±2-V V_{OD} and a maximum of ±3-V V_{OS} are measured (see Figure 3). Furthermore, a check on driver output-voltage balance between the differential output voltages is put in place to measure the change in these voltages (not to exceed 400 mV). The maximum limit of 400 mV most often is approached during transients when driver outputs are switching states.

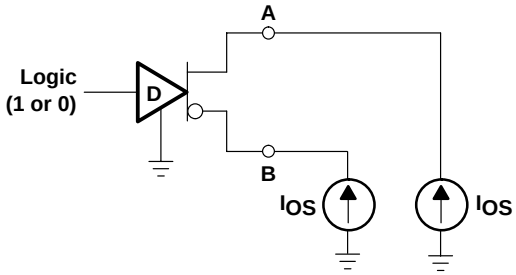


NOTES: A. $|V_{OD}| \geq 2$ V, $|V_{OS}| \leq 3$ V
B. $|\Delta V_{OD}| = ||V_{OD}| - |\overline{V_{OD}}|| \leq 0.4$ V
C. $|\Delta V_{OS}| = ||V_{OS}| - |\overline{V_{OS}}|| \leq 0.4$ V

Figure 3. Output-Voltage Test Circuit

Short-Circuit Output Current (I_{OS} Measured)

With the driver shorted to ground, the magnitude of the output current shall not exceed 150 mA, regardless of the state of the driver output (high or low) at the time of the short. This test ensures that the device is not destroyed by excessive current flowing through the output stage. Figure 4 shows the test circuit.

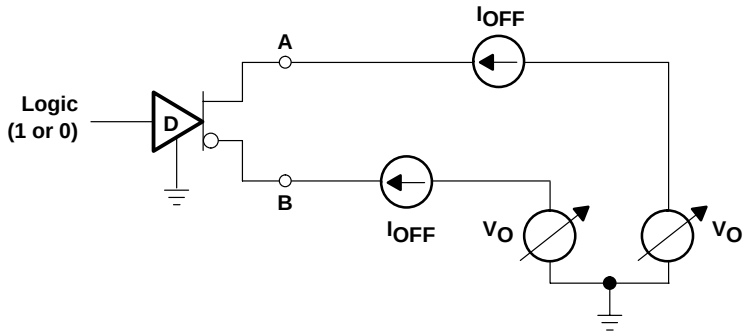


NOTE A: $|I_{OS}|$ to ground ≤ 150 mA

Figure 4. Short-Circuit Output-Current Test Circuit

Power-Off Measurement (I_{OFF} Measured; V_O Applied)

As shown in Figure 5, with the driver powered down, the magnitude of the output leakage current shall not exceed 100 μA for output voltages ranging from –0.25 V to 6 V. Currents higher than 100 μA can disrupt the bus potential and lead to erroneous data at the receiver.

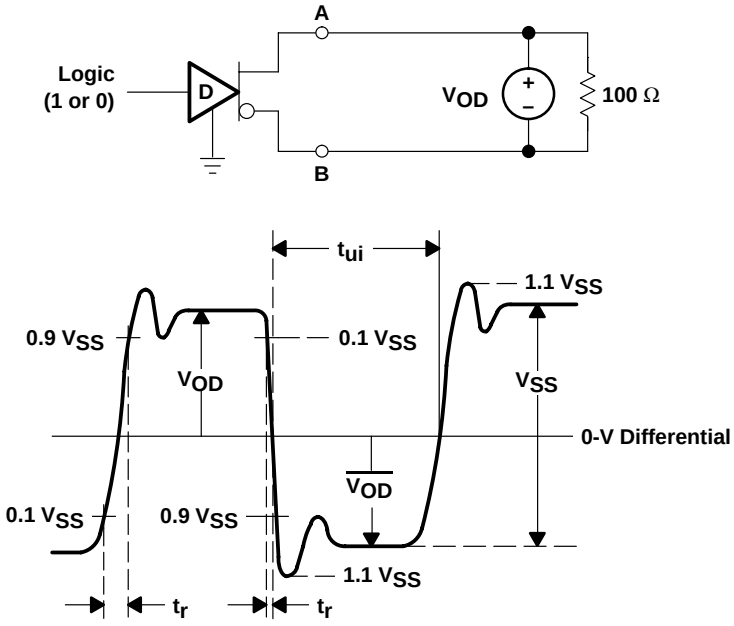


NOTE A: $|I_{off}| \le 100\ \mu A$ for $-0.25 \le V_O \le 6$ V

Figure 5. Power-Off Output-Current Test Circuit

Output-Signal Waveform (V_{OD} Measured)

Basically, this test ensures good signal quality on the bus. With a 100-Ω resistor across the differential output, the voltage should monotonically change between 10% and 90% of V_{SS} within a tenth of the unit interval, t_{ui}, or 20 ns, whichever is greater. Figure 6 shows the test circuit and resultant waveform. In addition, the resultant voltage shall not change more than 10% of V_{SS} after a transition has occurred (limits overshoots and undershoots).

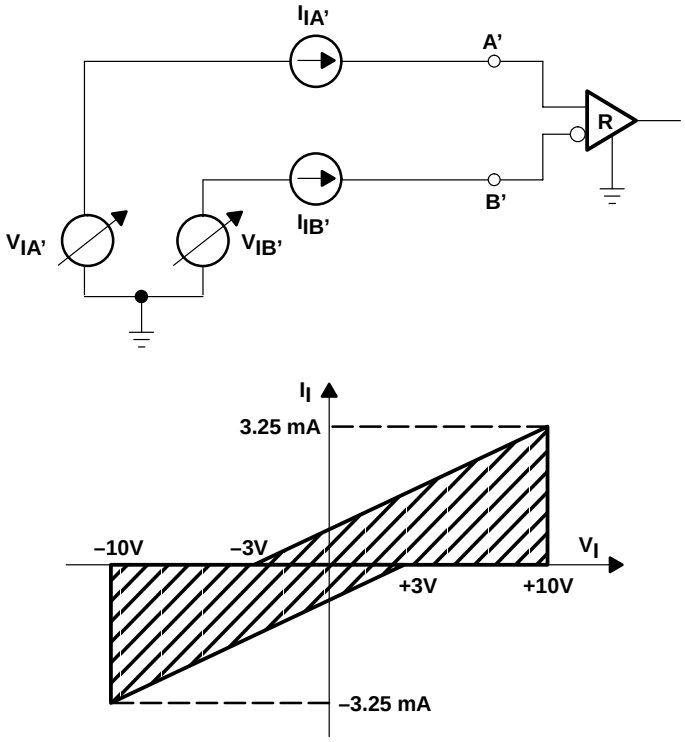


NOTES: A. t_{ui} = time duration of the unit interval
B. $V_{SS} = |V_{OD} - \overline{V_{OD}}|$
C. $2\ V \le |V_{OD}| \le 10\ V$

Figure 6. Test Circuit and Output-Signal Waveform

Input I/V Characteristics ($V_{IA'}$ and $V_{IB'}$ Applied; $I_{IA'}$ and $I_{IB'}$ Measured)

A maximum limit on the input characteristic must be placed on the receiver to ensure a maximum load on the bus when all ten receivers are placed on it. With the common-mode voltage $V_{IA'}$ ($V_{IB'}$) ranging from +10 V to –10 V while $V_{IB'}$ ($V_{IA'}$) is held to 0 V, the resultant input current should remain within the shaded region (see Figure 7) in both the power-on and power-off conditions. A device with input characteristics within the shaded region reveals that the input impedance is no smaller than 4 kΩ, as defined by the calculation. The inverse of the slope of the upper and lower bounds is exactly the minimum input impedance allowed for the input.

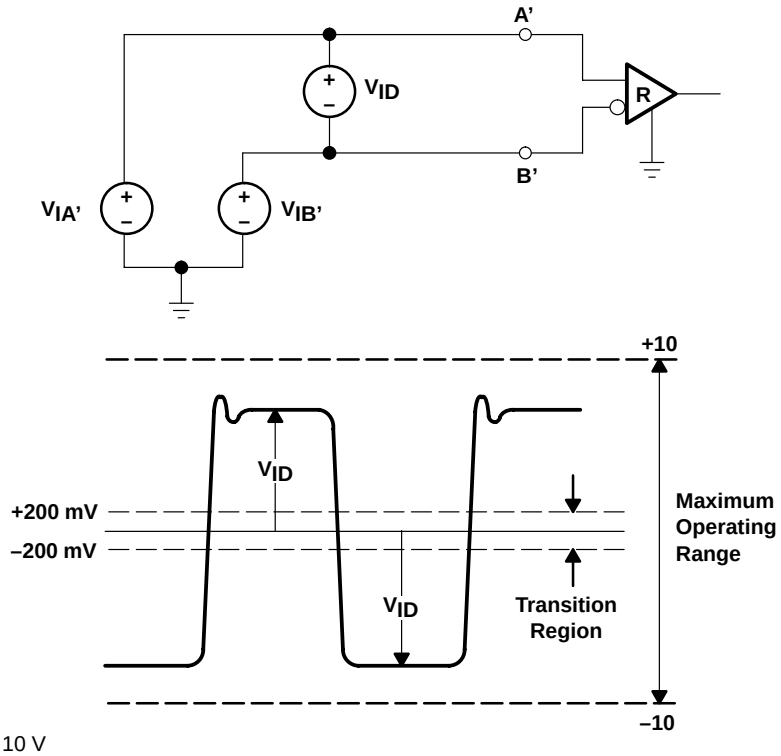


NOTE A: R = ΔV/ΔI = 13 V/3.25 mA = 4 kΩ

Figure 7. Input Receiver Test Circuit and I/V Plot

Input Sensitivity (V_{CM} , $V_{IA'}$ and $V_{IB'}$ Applied; V_{ID} Measured)

Figure 8 shows the test circuit used to determine a receiver's input sensitivity. To ensure functionality over the full common-mode range, suggested test voltages for both inputs and the purpose of the measurements are given in Table 1.



NOTE A: 200 mV < $|V_{ID}|$ < 10 V

Figure 8. Input-Sensitivity Test Circuit and Resultant Waveform

For a common-mode voltage varying from –7 V to 7 V, V_{ID} need not be greater than ±200 mV to correctly assume the intended state. As specified in the standard, the magnitude of the differential input voltage, V_{ID}, varying from 200 mV to 10 V, is required to maintain correct operation over this range.

Table 1. Input Sensitivity and Resultant Voltages of 422-Compliant Devices

APPLIED VOLTAGE		RESULTING V_{ID}	RESULTING V_{CM}	RECEIVER OUTPUT STATE	PURPOSE OF MEASUREMENTS
$V_{IA'}$	$V_{IB'}$				
+10 V	–2 V	+12 V	+4 V	Q	Ensures correct operation with maximum differential voltage supply
–10 V	+2 V	–12 V	–4 V	$\overline{Q}$	
+10 V	+4 V	+6 V	+7 V	Q	Ensures correct operation with maximum common-mode voltage supply
–10 V	–4 V	–6 V	–7 V	$\overline{Q}$	
+100 mV	–100 mV	+200 mV	0 V	Q	200-mV threshold test across common-mode voltage supply
–100 mV	+100 mV	–200 mV	0 V	$\overline{Q}$	
+7.1 V	+6.9 V	+200 mV	+7 V	Q	
–7.1 V	–6.9 V	–200 mV	–7 V	$\overline{Q}$	

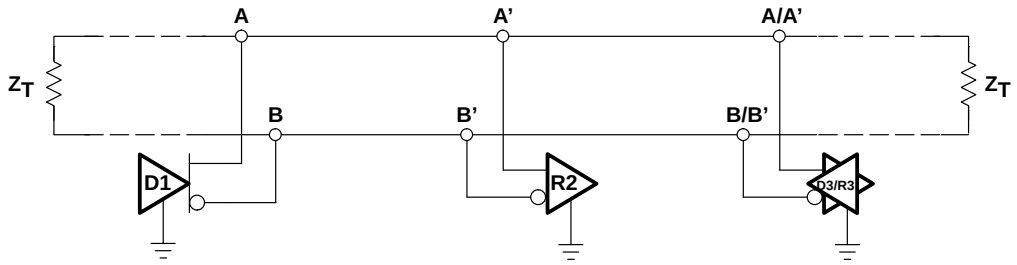
NOTES: 1. $|V_{IA'}|$ < 10 V, $|V_{IB'}|$ < 10 V (maximum input voltages to ensure correct operation)
2. $|V_{ID}|$ < 12 V (maximum input differential voltage without damaging device)
3. V_{CM} is measured as the arithmetic average of $V_{IA'}$ and $V_{IB'}$, or $(V_{IA'} + V_{IB'})/2$.

Cable Termination

Cable termination is required, unless the data rate of the application is less than 200 kbps or the signal rise/fall time at the load end of the cable is greater than four times the one-way cable delay. The latter rule-of-thumb typically is used to describe a system that does not behave like a transmission line. In most other applications, cable termination is recommended. Cable termination for a 422-compliant system always is placed at the load end of the cable. Two options for cable termination are recommended in the standard. The first option is to match the termination resistance to the characteristic impedance of the cable, Z_O, while the second option is to place an additional capacitor in series with the termination resistance for designers that are concerned with power dissipation. These two options are discussed in detail in the *Suggested Termination and Grounding Techniques* section.

Selected 485 Electrical Specifications

By comparing Figure 1 and Figure 9, it is evident that 422 and 485 system topologies are different. The 485 can operate in balanced digital multipoint systems, whereas the 422 can support only one driver per bus line (multidrop). Parameter values specified in 485 are similar to those specified in 422. Furthermore, 485-compliant receiver and driver electrical characteristics are specified such that they cover requirements of 422. This allows 485-compliant drivers and receivers to be used in most 422-compliant applications.



NOTES: A. D1 = driver
B. D3/R3 = transceiver
C. R2 = receiver
D. Z_T = termination impedance
E. Up to 32 U.L.s [receiver, driver (off state), transceiver]

Figure 9. 485 Balanced-Voltage Digital-Interface Circuit

Although 485 specifies that only one driver can talk at any given time (half-duplex operation), fault conditions might occur (caused by inadvertent shorts on output drivers or line contention). Therefore, 485-compliant devices must provide for this. For example, consider the case when driver D1 in Figure 9 is intended to send a signal to receiver R2, but driver D3 still is enabled. If the designer did not disable driver D3 before initiating the transmission, a fault condition occurs and erroneous data might be transmitted to receiver R2. This condition also is known as line contention (see *Summary Comparison of the Standards* section).

The maximum recommended cable length is about 1200 m. Usually, the amount of noise a designer is willing to tolerate is the deciding factor in choosing the cable length. The same relationship of speed versus cable length applies to 485-compliant systems, as well as to 422-compliant systems.

U.L. Concept (V_{IA} and V_{IB} Applied; I_{IA} and I_{IB} Measured)

As with the 422, a maximum limit on the I/V characteristic must be placed on the receiver, driver (off state), and transceiver to ensure a maximum load on the bus when all 32 U.L.s are utilized. With the voltage V_{IA} (V_{IB}) ranging from –7 V to 12 V, while V_{IB} (V_{IA}) is grounded, the resulting input current I_{IA} (I_{IB}) should remain within the shaded region in both power-on and power-off conditions (see Figure 10). A device with input characteristics that fall within the shaded region conforms to having a 1-U.L. characteristic. The 485 standard specifies the capability to sustain up to 32 U.L.s. The 485 often is thought of as a 12-kΩ load standard. Because the output current of the driver is dependent on loading, a design that requires a large number of stations (drivers, receivers, or transceivers) attached to the bus needs a larger load resistance to allow more connections. For example, a 0.5-U.L. transceiver can be placed up to 64 times on a bus, because this configuration complies with the maximum 32-U.L. specification.

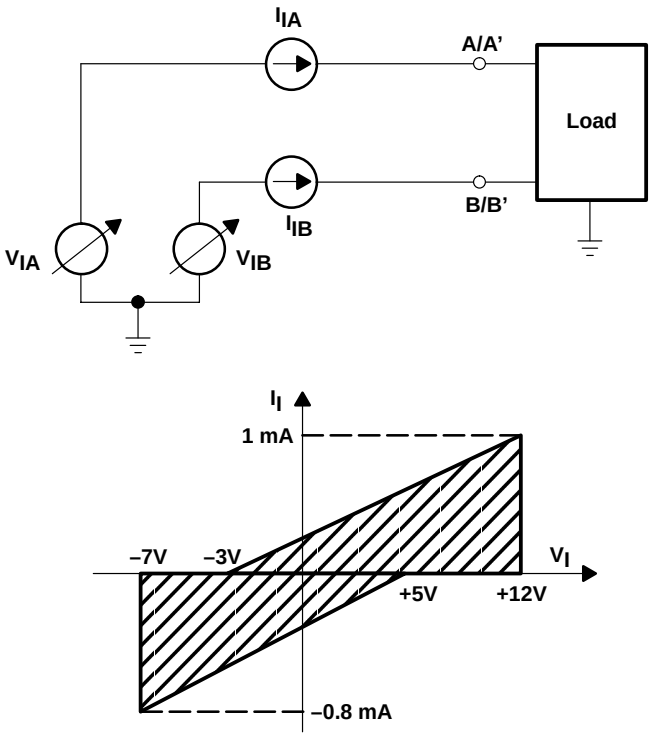
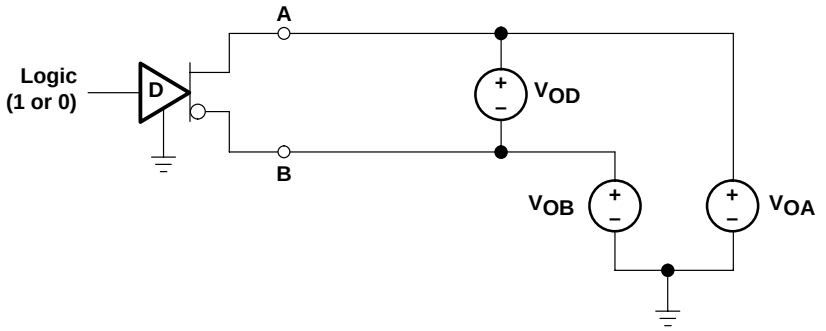


Figure 10. U.L. Test Circuit and I/V Relationship

Open-Circuit Output Voltage (V_{OD}, V_{OA}, and V_{OB} Measured)

The output voltage shall not exceed ±6 V under unloaded conditions, and the differential voltage generated will be no smaller than ±1.5 V and no greater than ±6 V. Figure 11 shows the test circuit used.

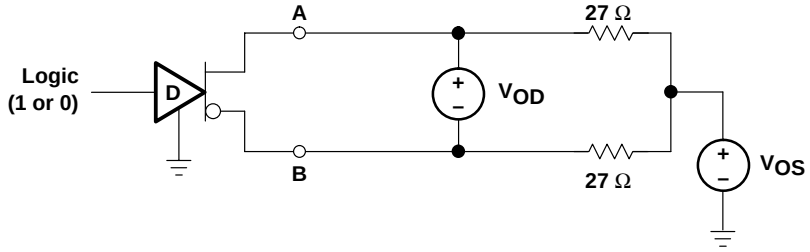


NOTES: A. $1.5\ V \le |V_{OD}| \le 6\ V$
B. $|V_{OA}| \le 6\ V$; $|V_{OB}| \le 6\ V$

Figure 11. Open-Circuit Test Circuit

Differential and Offset Output Voltage (V_{OD} and V_{OS} Measured)

Similar to the 422, 485 also specifies a minimum output voltage to ensure proper drive strength, but also places a maximum limit. Figure 12 shows the limitations that have been placed on the differential and offset voltages. It also shows the magnitude in the change in these voltages shall not exceed 200 mV.

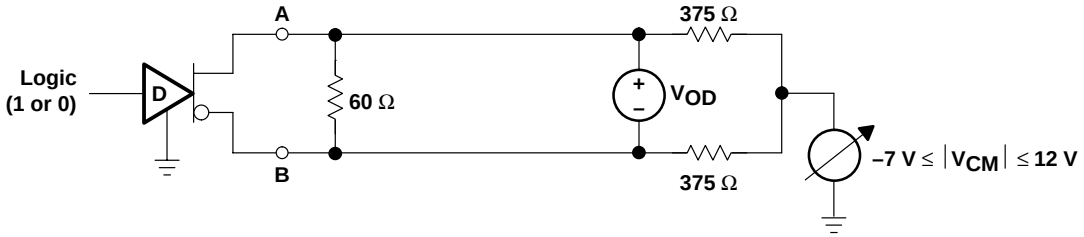


NOTES: A. $1.5\ V \le |V_{OD}| \le 5\ V$, and $|\Delta V_{OD}| = \left|\,|V_{OD}| - |\overline{V_{OD}}|\,\right| \le 0.2\ V$
B. $-1\ V \le |V_{OS}| \le 3\ V$, and $|\Delta V_{OS}| = \left|\,|V_{OS}| - |\overline{V_{OS}}|\,\right| \le 0.2\ V$

Figure 12. Output-Voltage Test Circuit

Differential Output Voltage With Common-Mode Loading (V_{OD} Measured; V_{CM} Applied)

With the test circuit shown in Figure 13, the magnitude of the differential output voltage shall fall within 1.5 V and 5 V.

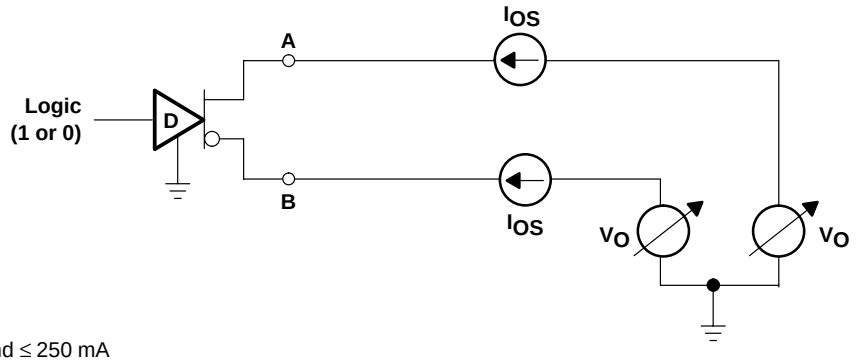


NOTE A: $1.5\ V \le |V_{OD}| \le 5\ V$

Figure 13. Output-Voltage Test Circuit With Common-Mode Loading

Short-Circuit Output Current (I_{OS} Measured; V_O Applied)

With the driver shorted to a voltage source that is varied from –7 V to 12 V, current shall not exceed 250 mA, and the driver shall not be damaged (see Figure 14). Texas Instruments incorporates into all its 485-compliant devices a thermal shutdown circuit that meets this requirement.



NOTE A: $|I_{OS}|$ to ground ≤ 250 mA

Figure 14. Short-Circuit Output-Current Test Circuit

Although the thermal shutdown circuitry limits the amount of current flowing from the output driver, complying with the full range from –7 V to 12 V for an indefinite time is a very stringent test. For customers seeking devices with various levels of robustness, TI offers products that comply fully (indeterminate time period and full voltage range) and partially with this specification. Partially compliant devices may limit the current over the full range, but cannot sustain the current over a long period of time. Another example of partial compliance is the capability to keep the current within specification for long periods, but at a smaller voltage range.

Output-Signal Waveform (V_{OD} Measured)

To ensure signal quality, 485 also places a constraint on the output-signal waveform. The output-signal waveform is identical to the one described for the 422, but a different test circuit is necessary (see Figure 15). The output voltage should change monotonically between 0.1 V_{SS} and 0.9 V_{SS} within 0.3 t_{ui}. Thereafter, the output voltage shall not change more than 10% of V_{SS}, and $|V_{OD}| \leq 5$ V.

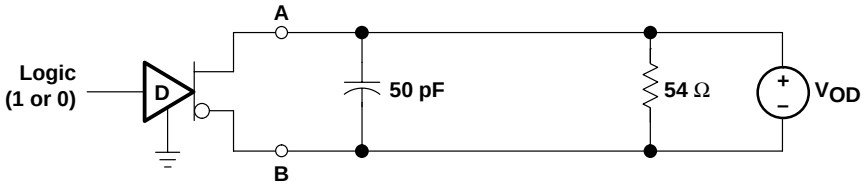


Figure 15. Output-Signal Test Circuit

Input Sensitivity (V_{CM}, $V_{IA'}$ and $V_{IB'}$ Applied; V_{ID} Measured)

Using the same test circuit as in 422, Table 2 shows the operating voltage extremes of the receiver and the purpose of each measurement.

Table 2. Input Sensitivity and Resultant Voltages of 485-Compliant Devices

APPLIED VOLTAGE		RESULTING V_{ID}	RESULTING V_{CM}	RECEIVER OUTPUT STATE	PURPOSE OF MEASUREMENT
$V_{IA'}$	$V_{IB'}$				
–7 V	–6.8 V	–200 mV	–6.9 V	$\overline{Q}$	Minimum V_I at extreme – V_{CM}
+12 V	+11.8 V	+200 mV	+11.9 V	Q	Minimum V_I at extreme + V_{CM}
–7 V	–2 V	–5 V	–4.5 V	$\overline{Q}$	Maximum V_I at extreme – V_{CM}
+12 V	+7 V	+5 V	+9.5 V	Q	Maximum V_I at extreme + V_{CM}

Suggested Termination and Grounding Techniques

When designing a system that utilizes drivers, receivers, and transceivers that comply with 422 or 485, proper cable termination is essential for highly reliable applications with reduced reflections in the transmission line. Because 422 allows only one driver on the bus, if termination is used, it is placed only at the end of the cable near the last receiver. In general, 485 requires termination at both ends of the cable.

Factors to consider when determining the type of termination usually are performance requirements of the application and the ever-present factor, cost. The different types of termination techniques discussed are unterminated lines, parallel termination, ac termination, open-line fail-safe termination, open/shorted-line fail-safe termination, and multipoint termination. Laboratory waveforms for each termination technique (except multipoint termination) illustrate the usefulness and robustness of 422 (and, indirectly, 485). Similar results can be obtained if 485-compliant devices and termination techniques are used. For laboratory experiments, 100 feet of 100-Ω, 24-AWG, twisted-pair cable (Bertek) was used. A single driver and receiver, TI AM26C31C and AM26C32C, respectively, were tested at room temperature with a 5-V supply voltage. Two plots per termination technique are shown. In each plot, the top waveform is the driver input and the bottom waveform is the receiver output. To show voltage waveforms related to transmission-line reflections, the first plot shows output waveforms from the driver at the start of the cable, while the second plot shows the waveforms related to the receiver inputs at the end of the cable.

Resistor and capacitor (if used) termination values are shown for each laboratory experiment, but vary from system to system. For example, the termination resistor, Z_T, must be within 20% of the characteristic impedance, Z_0, of the cable and can vary from about 90 Ω to 120 Ω. However, suggestions for determining values for resistors R_{DN}, R_{UP}, and R_S are provided.

No Termination

Figure 16 shows a configuration with no termination. Figures 17 and 18 show that, although reflections are present at the receiver inputs at a data signaling rate of 200 kbps with no termination, the 422-compliant receiver reads only the input differential voltage and produces a clean signal at the output.

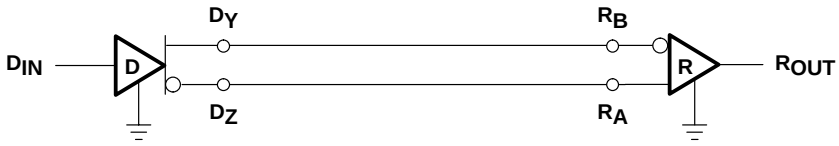


Figure 16. Differential Unterminated Configuration

- Advantages
  - Driver is only required to source a minimal amount of current to produce a signal at the receiver.
  - Minimizes the driver's on-chip power dissipation
  - Ensures that the receiver's output is in a known state if the receiver internally features open-line fail safe
- Disadvantage
  - Signal reflections due to mismatched line impedance at high data signaling rates (should be used only in applications with data rates ≤200 kbps and short distances) (If $t_r > 4t_{delay}$, the cable is not considered a transmission line.)

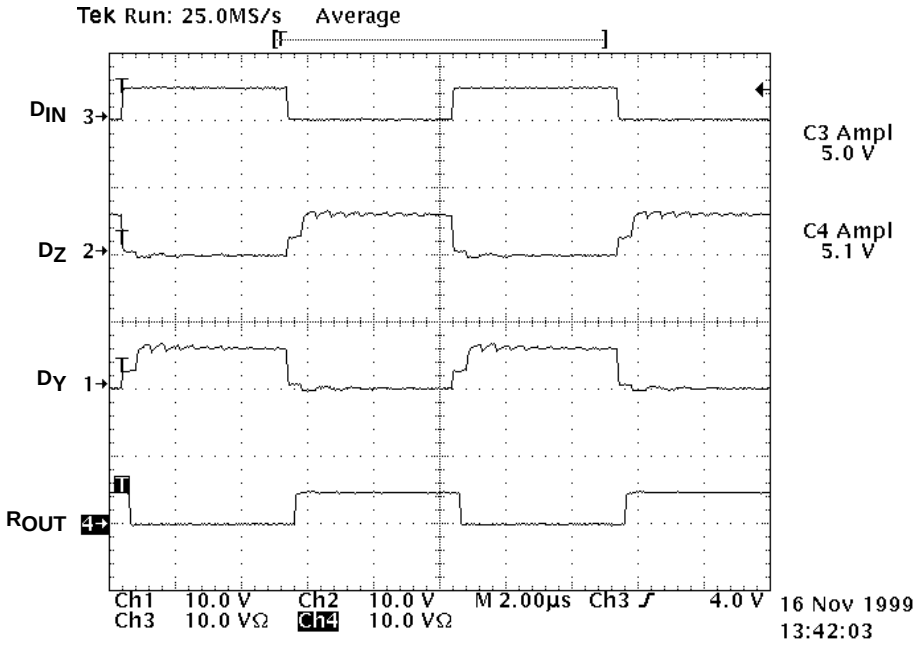


Figure 17. Differential Unterminated-Driver Output Waveforms

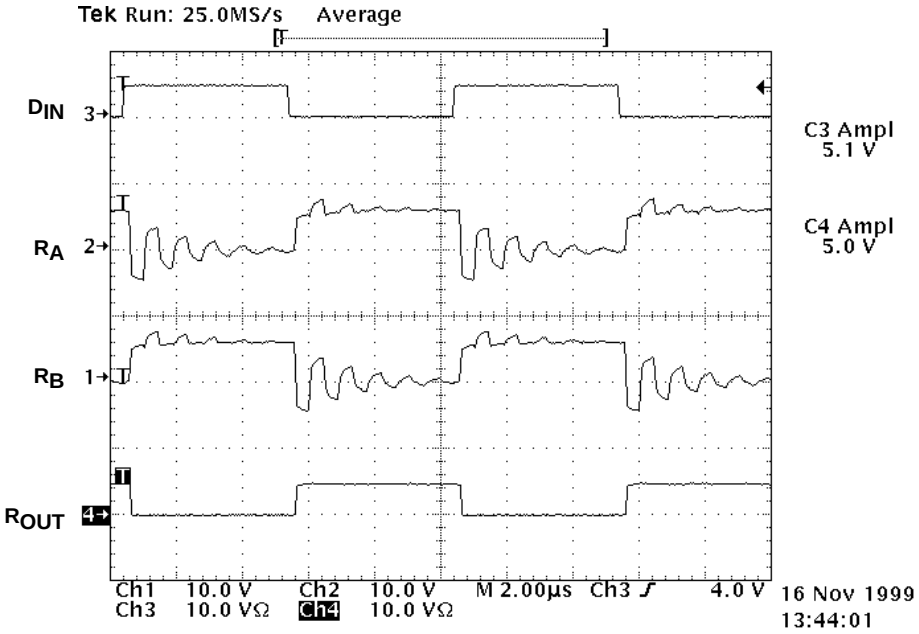
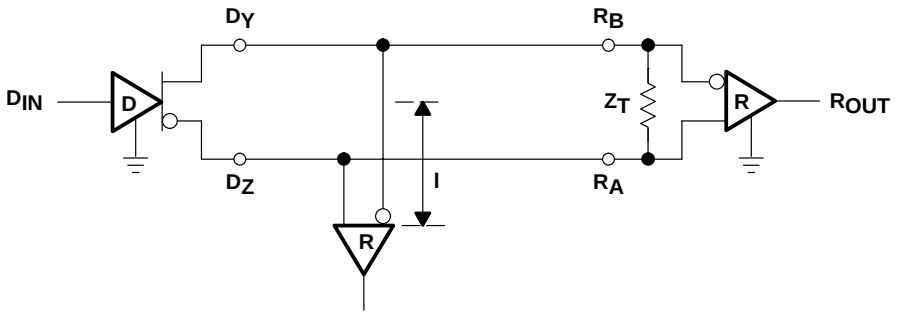


Figure 18. Differential Unterminated-Receiver Input Waveforms

Parallel Termination

Figure 19 shows a typical configuration using an impedance termination across the differential inputs at the far-end receiver. As shown in Figures 20 and 21, parallel termination ensures that there are no impedance mismatches and eliminates reflections. A termination resistance of 100 Ω was applied, and only one receiver was used in this experiment, while transmitting at a data signaling rate of 1 Mbps.



NOTE A: $Z_T = Z_O$

Figure 19. Differential Parallel-Terminated Configuration

- Advantages
  - Elimination of reflections: higher data rates and longer cables
  - Multidrop applications are also supported.
- Disadvantages
  - Long stub lengths (l) reintroduce reflections.
  - Increase in driver's power dissipation (when compared to the unterminated case)
  - Receiver's output is not ensured when the driver is idle or placed in the high-impedance state.

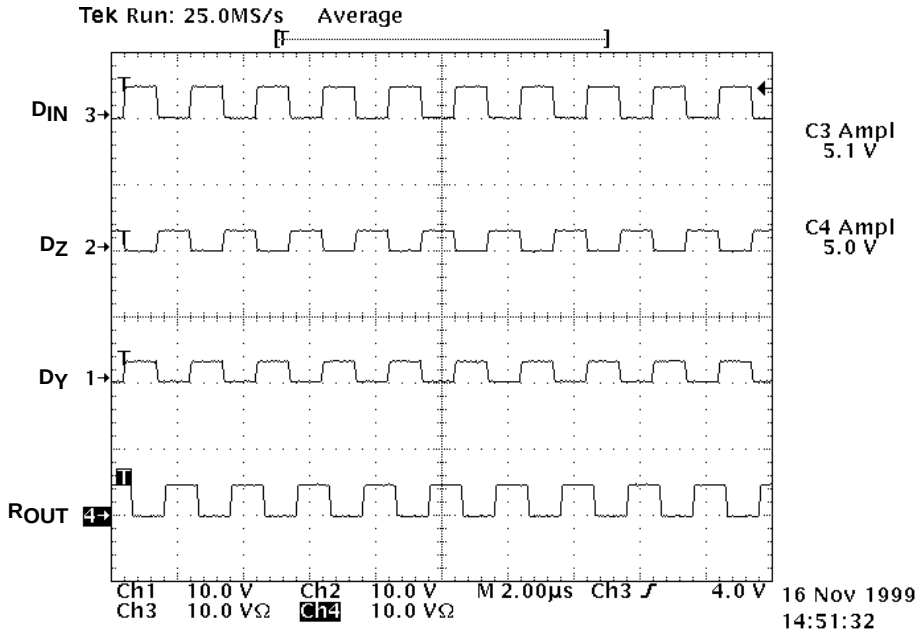


Figure 20. Differential Parallel-Terminated Driver Output Waveforms

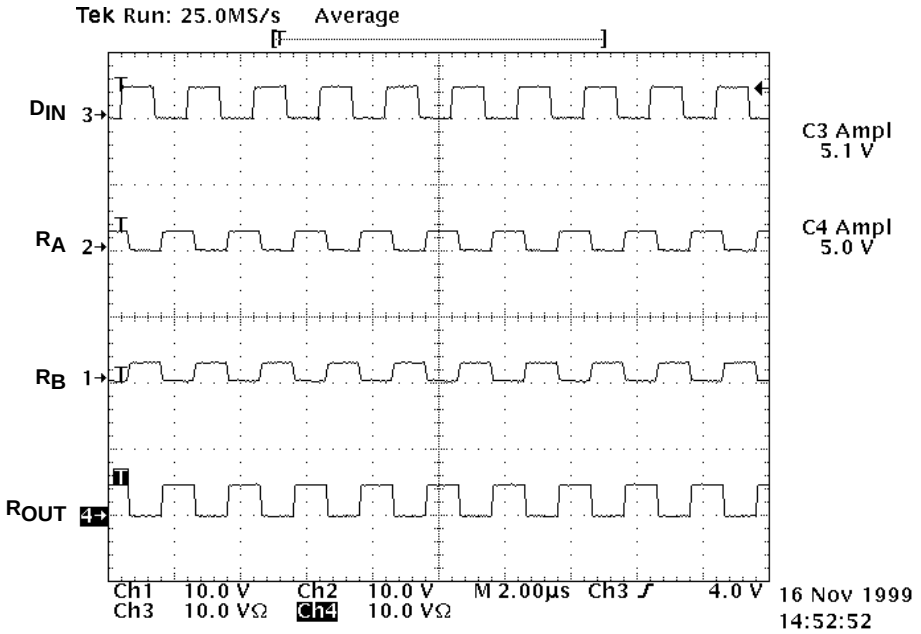
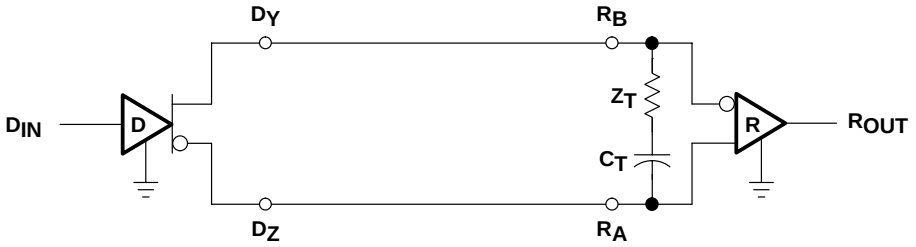


Figure 21. Differential Parallel-Terminated Receiver Input Waveforms

AC Termination

Because the differential outputs are complementary when the driver is activated, one output is in the high state, while the other is in the low state. Current flows from the high-state output to the low-state output through the termination resistor, as in the parallel configuration. A capacitor and resistor are used for ac termination to eliminate the dc current path from one differential output to the other. Figure 22 shows the connectivity. However, this added RC time-constant delay significantly reduces transmission speeds. Figures 23 and 24 illustrate acceptable receiver input and output waveforms using an ac termination of Z_T = 100 Ω and a 1000-pF capacitor. The data rate was limited to 200 kbps in laboratory measurements. If a 485-system with multiple drivers is used, place another Z_T and C_T across the balanced line at the other end of the cable.



NOTES: A. $Z_T = Z_O$
B. Choose C_T so that the resultant RC time constant is small compared to the unit interval.

Figure 22. Differential AC-Terminated Configuration

- Advantages
  - Driver power dissipation is decreased compared to parallel termination, but not as much as in the unterminated case.
  - Line reflections are reduced.
  - Ensures that the receiver's output goes to a known state if the receiver internally features open-line fail-safe
- Disadvantage
  - Limitation on maximum data signaling rate and cable distance due to RC time constant (typically used on low-speed control lines)

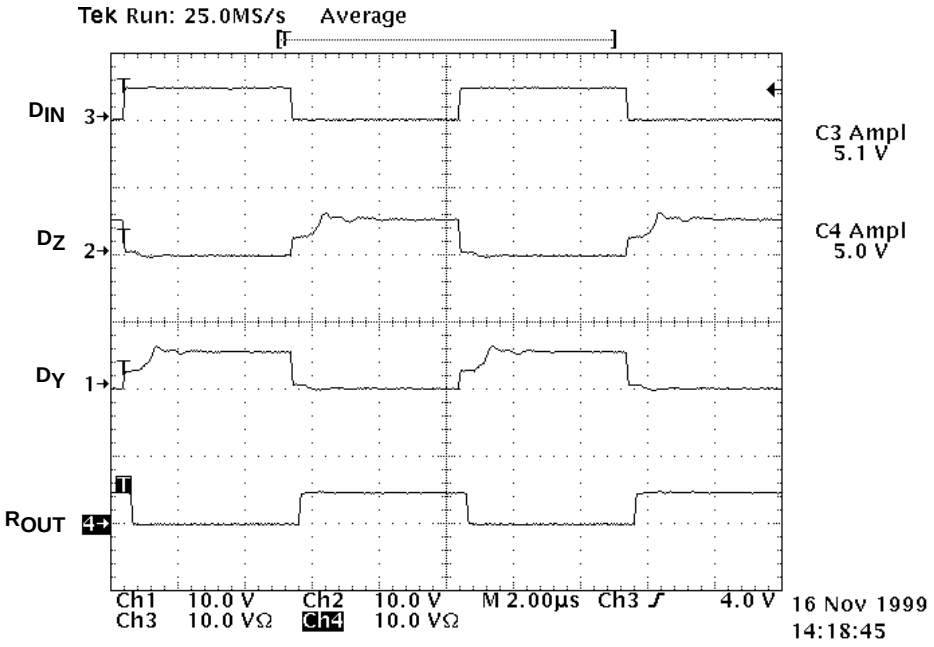


Figure 23. Differential AC-Terminated Driver Output Waveforms

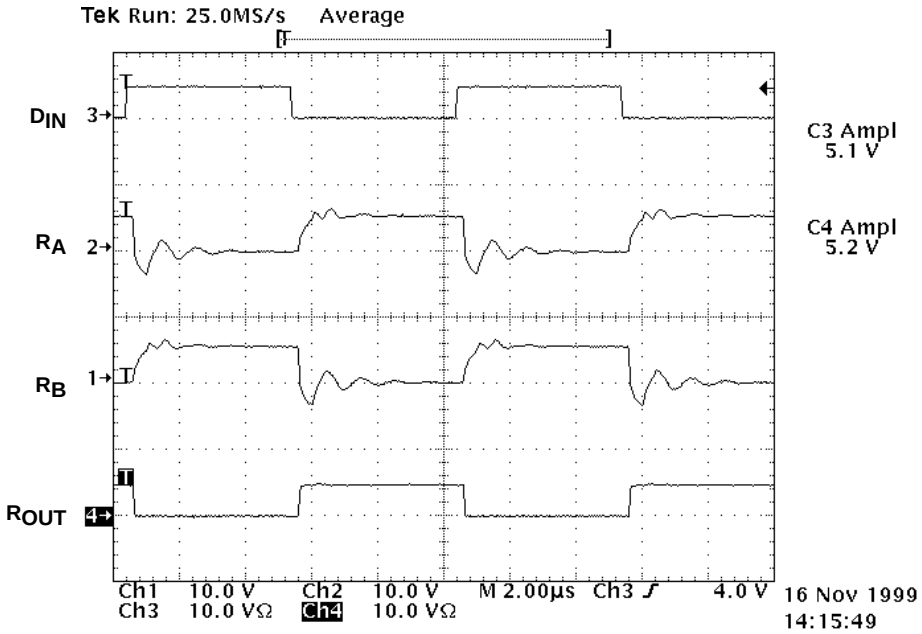


Figure 24. Differential AC-Terminated Receiver Input Waveforms

Open-Line Fail-Safe Termination

Typically, differential receivers are equipped internally with open-line fail-safe circuitry. Therefore, if the driver driving the receiver were placed in the high-impedance state, the receiver's output eventually would go to a known state. However, if a termination resistance is used, as is commonly done, the receiver no longer supports open-line fail-safe. Therefore, external pullup and pulldown resistors must be used (see Figure 25).

NOTES: A. $Z_T = Z_0$
B. Choose R_{UP} and R_{DN} to be equal, so that at least 200 mV develops across the receiver differential input.

Figure 25. Differential Open-Line Fail-Safe-Terminated Configuration

If a 485-compliant system with multiple drivers is employed, another Z_T should be placed across the balanced line near the driver at the other end of the cable. For proper impedance matching, Z_T must be increased, because the equivalent reduced resistance seen by the driver is the resistive ladder shown in Figure 25, with R_{UP} shorted to ground (under ac conditions).

For laboratory experiments, the pullup and pulldown resistors were 820 Ω each, while Z_T = 100 Ω. The equivalent resistance of the R_{UP}, R_{DN}, and Z_T, as seen by the driver, does not exactly match the characteristic impedance, Z_0, of the cable, but still should be within 20% of its value. Figures 26 and 27 show that, at a data signaling rate of 1 Mbps, and with the proper termination, the waveforms produced are acceptable.

- Advantage
  - Forces a V_{ID} of at least 200 mV across the receiver's inputs to ensure a known state at the output when the driver is idle or disconnected
- Disadvantages
  - Increased driver loading increases the driver's output power consumption.
  - High power dissipation
  - Fewer U.L.s available for receivers

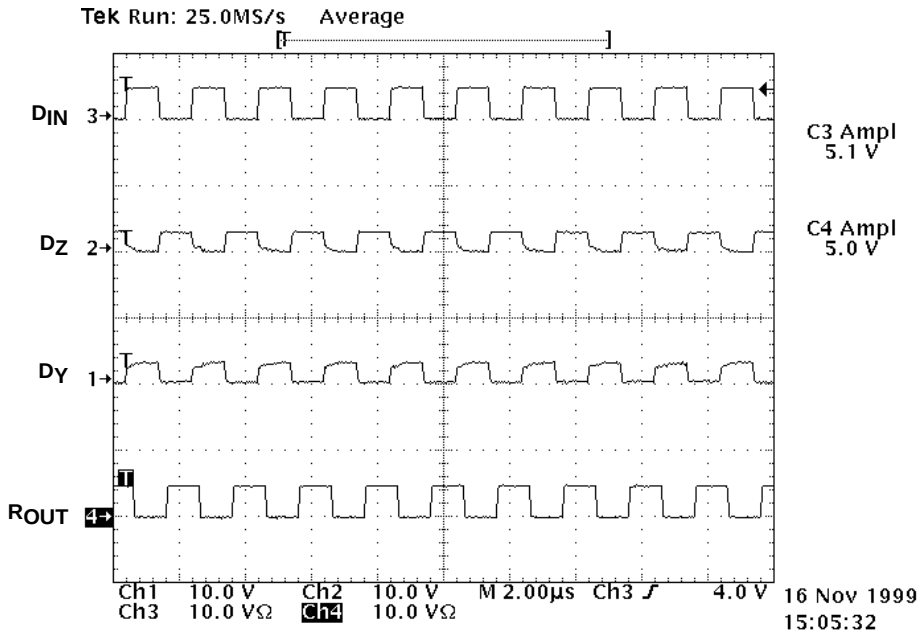


Figure 26. Differential Open-Line Fail-Safe-Terminated Driver Output Waveforms

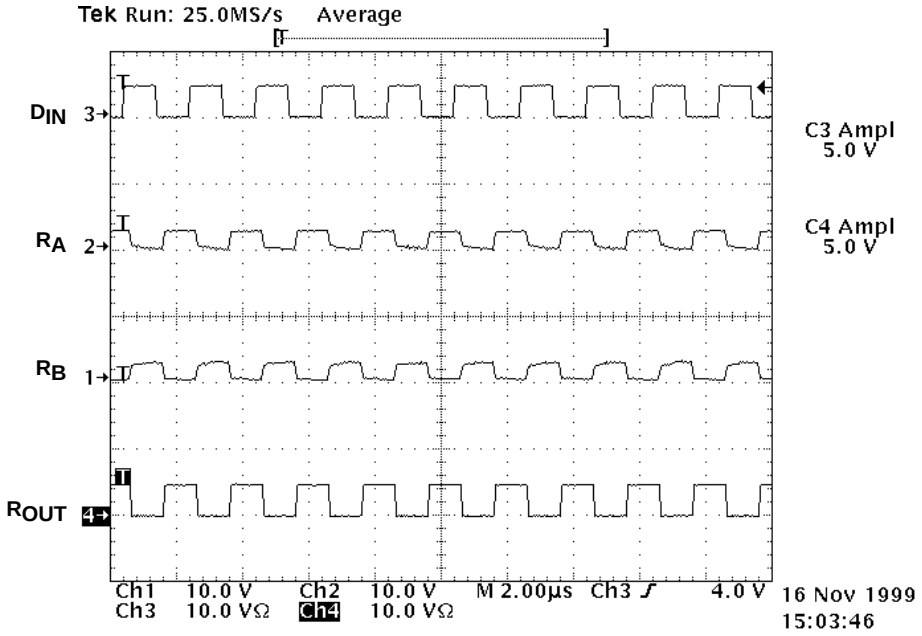


Figure 27. Differential Open-Line Fail-Safe-Terminated Receiver Input Waveforms

Open-Line and Shorted-Line Fail-Safe Termination

In the previous configuration, if there is a short across the differential output somewhere along the cable, 0 V is seen by the receiver and, subsequently, cannot determine in what state its output should be. Figure 28 shows that by adding extra resistance across the receiver inputs, this problem is eliminated.

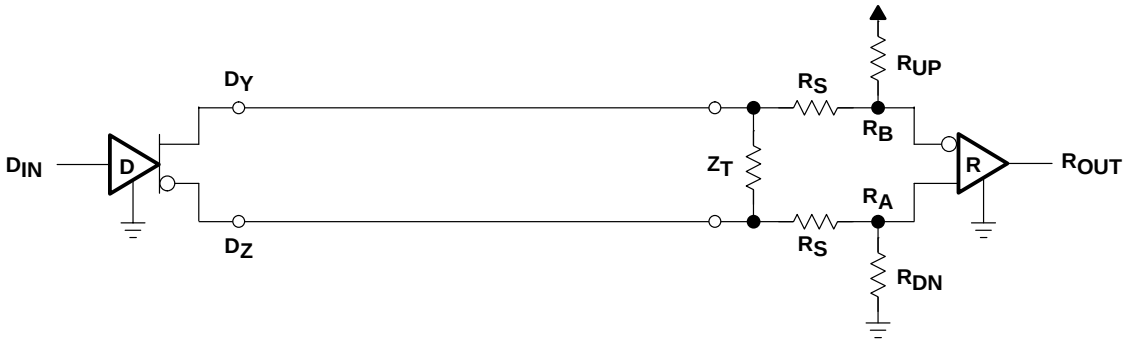


Figure 28. Differential Open-/Shorted-Line and Fail-Safe-Terminated Configuration

This configuration is intended for harsh environments. Several restrictions in calculating termination resistor values apply. First, if a short is detected on the bus (thereby negating Z_T), an equivalent resistor value twice that of R_S still should be present between the differential input of the receiver. Choose R_S, so that R_{UP} and R_{DN} have no difficulty forcing the inputs apart by at least 200 mV. Second, once the bus line goes into high impedance, an effective resistance of Z_T and two R_S in series is seen by the receiver, with R_{UP} pulling one input to V_{CC} and R_{DN} pulling the other input to ground. Choose R_{UP} and R_{DN} to efficiently develop a voltage of at least 200 mV across the receiver input. The last constraint is that the characteristic impedance of the transmission line should equal Z_T in parallel with twice the sum of R_S and R_{UP} (assuming $R_{UP} = R_{DN}$).

If a 485-compliant system with multiple drivers is employed, another Z_T should be placed across the balanced line at the end of the cable. For proper impedance matching, it is necessary to increase Z_T because the equivalent reduced resistance seen by the driver is the resistive ladder shown in Figure 28, with R_{UP} shorted to ground (under ac conditions).

For laboratory experiments, R_{UP} and R_{DN} are 2 kΩ each, R_S = 100 Ω, and Z_T = 100 Ω. The equivalent resistance of the resistor network of R_{UP}, R_{DN}, twice R_S, and Z_T, as seen by the driver, does not match exactly the characteristic impedance, Z_0, of the cable, but should be within 20% of its value. Figures 29 and 30 show excellent waveforms, with a data signaling rate of 1 Mbps.

- Advantages
  - Provides open-line and shorted-line fail-safe configuration
  - Receiver may be able to withstand a higher common-mode voltage range.
- Disadvantages
  - More costly
  - Not applicable with transceivers because R_S also would be in the output path of the driver

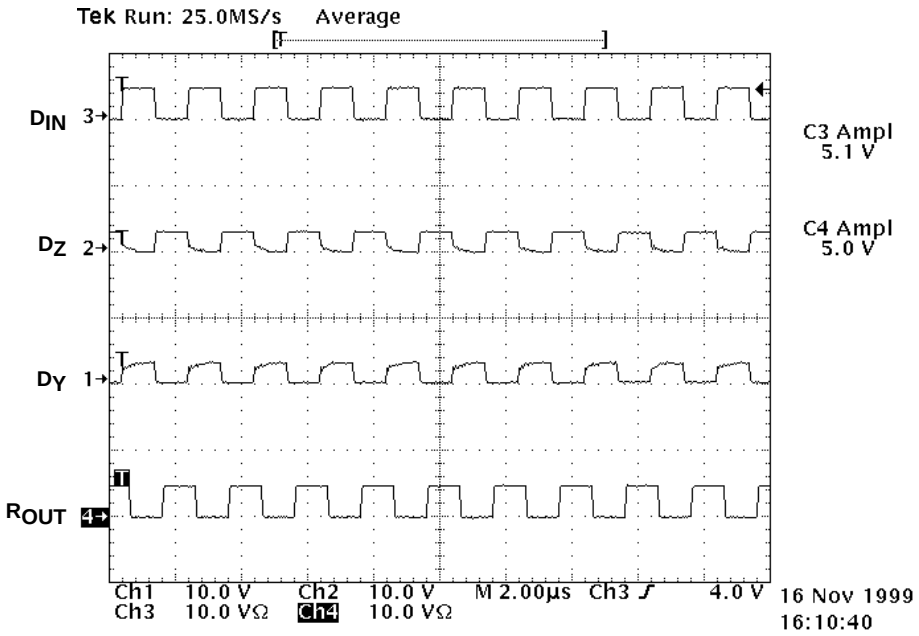


Figure 29. Differential Open-/Shorted-Line Fail-Safe-Terminated Driver Output Waveforms

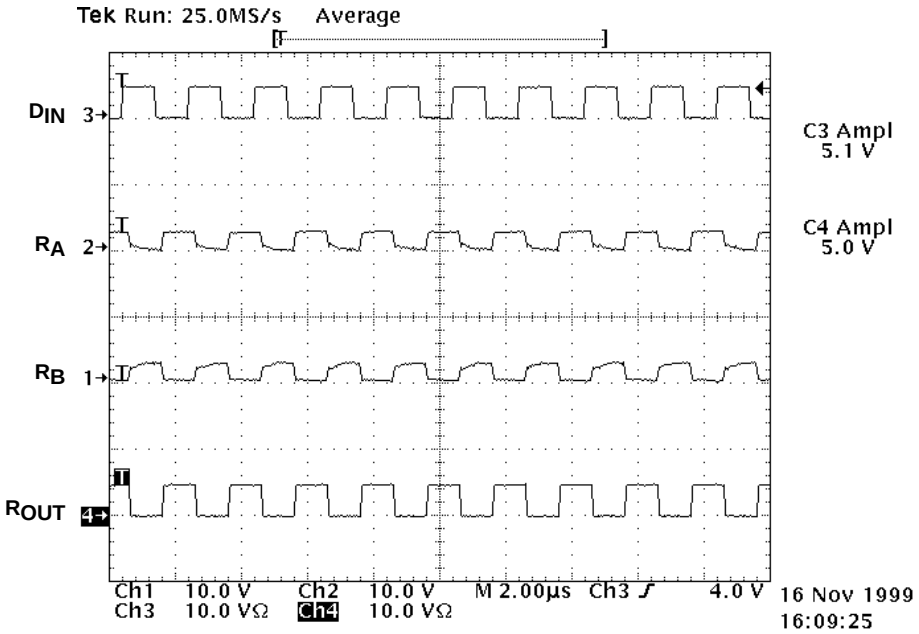
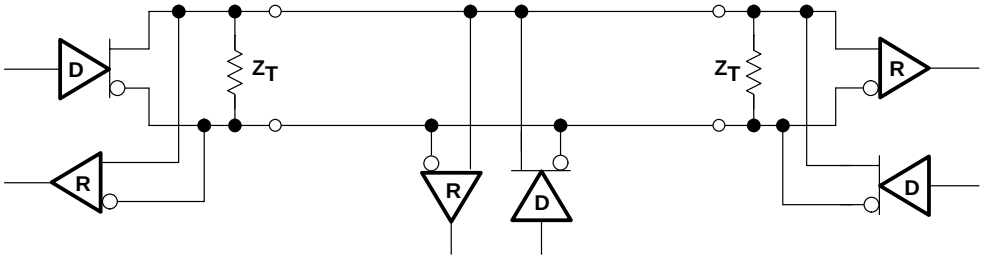


Figure 30. Differential Open-/Shorted-Line Fail-Safe-Terminated Receiver Input Waveforms

Multipoint Termination

Multipoint configurations are supported by 485, but not 422. Figure 31 shows a typical 485-compliant configuration, with a transceiver at both ends of the cable and drivers/receivers placed along the length of the cable. 485 requires termination at both ends of the cable (see Figure 31). No waveforms are provided for this configuration, but performance similar to that of the parallel-termination case can be expected.



NOTE A: $Z_T = Z_O$

Figure 31. Differential Multipoint-Terminated Configuration

- Advantages
  - Same as parallel termination
  - Optimum signal quality
- Disadvantage
  - Same as parallel termination, but two termination resistors are required, one at each end of the cable, which adds more loading to the drivers.

Ground Connections

All 422- and 485-compliant system configurations shown up to this point do not have incorporated signal-return paths to ground. Obviously, having a solid ground connection so that both receivers and drivers can talk error free is imperative. Figure 32 shows how to make this connection and recommends adding some resistance between logic and chassis ground to avoid excess ground-loop currents. Logic ground does not have any resistance in its path from the driver or receiver. A potential problem might exist, especially during transients, when a high-voltage potential between the remote grounds could develop. Therefore, some resistance between them is recommended.

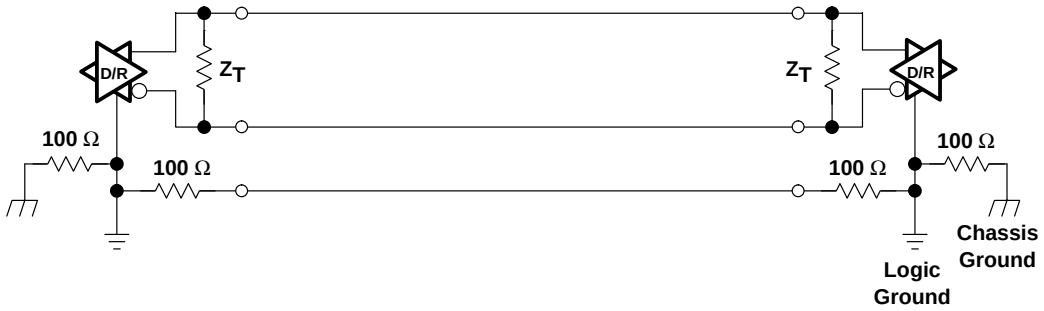


Figure 32. Recommended Grounding Configuration

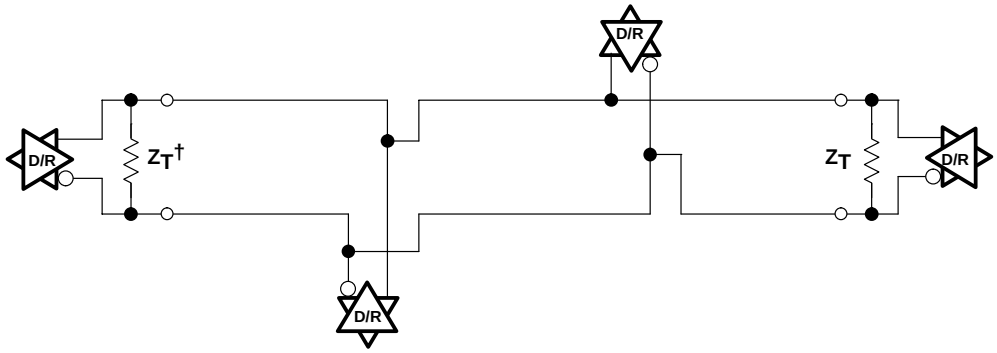
Typical System Configurations

This section presents a general idea about connecting balanced differential drivers, receivers, and transceivers in different situations. Properly connecting the devices greatly reduces reflections.

The following discussions on system configurations apply only to 485-compliant system designs. Conversion to a 422-compliant system is straightforward, knowing that the termination impedance, Z_T, is placed only once in close proximity to the last receiver at the end of the cable farthest from the driver. Also, only one driver is required, with up to nine additional receivers allowed in a 422-compliant system design.

General System Configuration

The most widely used connectivity scheme is called daisy-chaining. In this topology, each station is attached successively as close to the input/output as possible (see Figure 33). The idea is to make the main bus seem like only one transmission line.

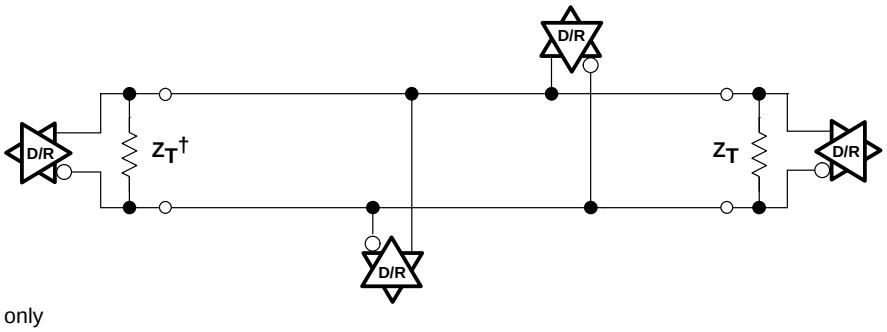


† 485-compliant system only

Figure 33. Daisy-Chain Connection

Backbone Configuration

Another popular connection scheme (shown in Figure 34) is connecting stations directly to the main bus (referred to as a backbone). To reduce line reflections, it is essential to keep the stubs (cable distance from main bus line) as short as possible. Again, the intent is for the driver to see only one transmission line.



† 485-compliant system only

Figure 34. Stub Cables Connected to the Main Backbone

Point-to-Point Configuration

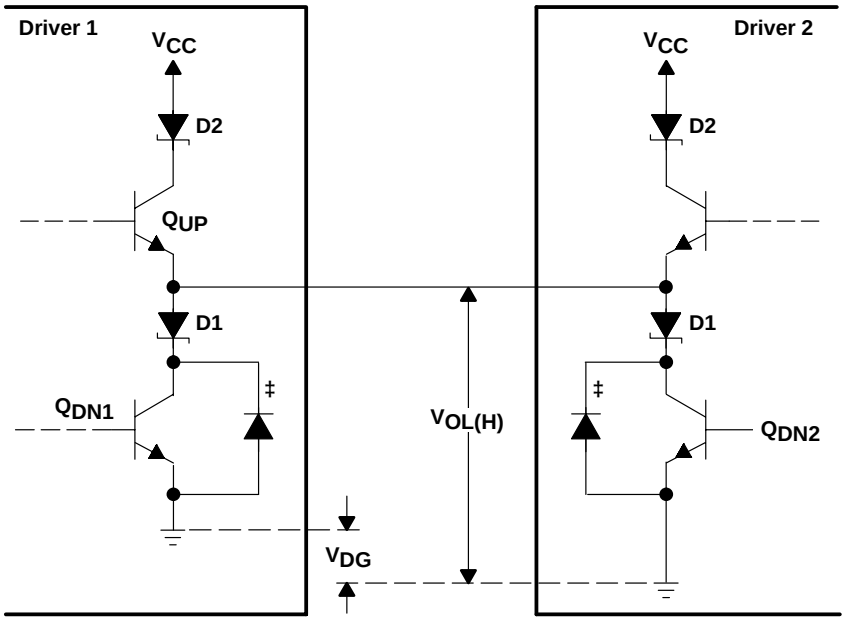
Point-to-point connectivity, in its simplest form of data transmission, is shown in Figure 35.

† 485-compliant system only

Figure 35. Point-to-Point Connection

Summary Comparison of the Standards

As discussed previously, 422 and 485 have similar requirements. 485-compliant drivers and receivers generally are interchangeable with those compliant to 422, but the reverse is not necessarily true. There are at least three major problems for 422-compliant drivers used in multipoint applications: common-mode range, line contention, and output drive current. Consider the case when at least two 485-compliant drivers are connected to a transmission line (see Figure 36). For simplicity, only two drivers are shown.



‡ Parasitic diode

Figure 36. Two 485 Drivers Connected to a Bus

Common-Mode Range

Because of Schottky diode D1, the parasitic diode (formed from the epitaxial layer to the substrate) cannot turn on if its output is pulled below its reference ground by $V_{DG} > 0.7$ V. Likewise, using Schottky diode D2 (along with D1) provides a common mode range of –7 V to 12 V, which is 7 V from either supply rail. 422-compliant drivers do not have these Schottky diodes incorporated into their circuitry, so only 0.25 V to 6 V is specified in the standard.

Line Contention

Line contention, as discussed previously, is caused when two or more drivers are turned on at the same time. For example, if Q_{UP} of driver 1 is turned on while Q_{DN2} of driver 2 also is turned on, a line-contention situation arises. Typically, 422-compliant drivers do not have line-contention protection built in because only one driver is present. 485 does not state that line-contention circuitry is required, but most drivers have what is called thermal shutdown circuitry that protects against line contention. Thermal shutdown disables the output driver when it senses a high temperature, and turns it back on after the device cools. If line contention still is present after the driver is enabled, thermal shutdown disables the driver again as soon as the temperature reaches a certain point. The output cycles in and out of thermal shutdown indefinitely until line contention no longer is present.

The problem with line contention is exacerbated when the ground potential between the remote grounds is stretched to its maximum limit of ±7 V (V_{DG} as shown in Figure 36). If Q_{DN2} is connected to the ground that is 7 V lower than the other remote ground, a potential close to +12 V could exist on the output of Q_{DN2} (assuming $V_{CC} = 5$ V). Now, consider the case where both Q_{DN1} and Q_{DN2} are turned on. If Q_{DN2} is connected to the ground that is 7 V higher than the other remote ground, a potential close to –7 V could exist on the output of Q_{DN2}. The 485 standard, as noted, limits the current out of the output when a voltage ranging from –7 V to 12 V is applied. Therefore, indirectly, the standard does require the addressing of line contention by limiting the output current.

Drive Current

Because 485 requires two termination resistors, but 422 requires only one termination resistor, 485 outputs typically are stronger. Furthermore, 422 allows driving up to 10 4-kΩ loads (equivalent to 400 Ω), while 485 allows driving up to 32 12-kΩ loads (equivalent 375 Ω). Therefore, with the same output drive strength, a 485-compliant driver can handle triple the number of loads.

Table 3 summarizes the main differences between 422 and 485; Table 4 summarizes attributes for each termination technique discussed.

Table 3. Summary Comparison of 485 and 422 Specifications

PARAMETER	422	485	UNIT
Number of drivers and receivers	1 driver 10 receivers	32 U.L.s	
Maximum theoretical cable length	1200	1200	m
Maximum data rate	10	10	Mbps
Maximum common-mode voltage	±7	12 to –7	V
Driver differential output level	$2 \le \lvert V_{OD} \rvert \le 10$	$1.5 \le \lvert V_{OD} \rvert \le 5$	V
Driver load	≥100	≥60	Ω
Driver output short-circuit current limit	150 to GND	150 to GND 250 to –7 V or 12 V	mA
High-impedance state, power off	60	12	kΩ
Receiver input resistance	4	12	kΩ
Receiver sensitivity	±200	±200	mV

Table 4. Summary of Termination Techniques

TECHNIQUE	POWER DISSIPATION	OPEN-LINE FAIL-SAFE	SHORTED-LINE FAIL-SAFE	SPEED	SIGNAL INTEGRITY
No termination	Low	Supported if available on receiver	Not supported	Low	Poor at high speeds
Parallel termination	Medium	Not supported	Not supported	High	Excellent
AC termination	Low	Supported if available on receiver	Not supported	Medium	Good
Open-line fail-safe termination	High	Supported	Not supported	High	Excellent
Open-line and shorted-line fail-safe termination	High	Supported	Supported	High	Excellent
Multipoint termination	Medium	Not supported	Not supported	High	Excellent

Conclusion

Although similarities exist between 422 and 485, board designers must consider distinct differences between devices specified for one standard or the other. This application report has outlined the major differences and provided suggested connection schemes. 485-compliant devices can be used in 422-compliant systems, but the opposite is not true.

TI offers a variety of devices that meet or exceed requirements of 422 and 485. TI's main competitive advantage is its extensive selection of bipolar and BiCMOS differential devices that are available at competitive prices, allowing the board designer to reduce system costs. For a complete listing of available devices from each standard, data sheets are available on the Internet at http://www.ti.com under interface products.

Frequently Asked Questions

1. What is TI's most popular 422/485 device?

   The single driver/receiver pair SN75ALS176B currently is the best-selling device, because of its high-speed capability (up to 35 Mbps) and competitive price offering.

2. How do 422- and 485-compliant devices compare with TI's LVDS (also known as 644) products?

   422- and 485-compliant devices have been in existence for many years and are in their mature life cycle. LVDS is the new balanced differential data-transmission scheme that operates at 3.3-V supply, while the older technologies operate at 5 V. Smaller voltage swings, smaller input sensitivity, and higher bandwidth on LVDS are some of the major parameter differences.

3. Can 485-compliant devices be used in 422-compliant applications?

   Yes, but the opposite is not true.

4. What is the maximum cable length for a given data signaling rate?

   This is discussed in the application section of the TI *Data Transmission Circuits Data Book,* literature number SLLD001, and is not within the scope of this application report. In general, the longer the cable, the slower the speed, because cable lengths and signaling speeds are inversely proportional.

Glossary

BiCMOS	Bipolar and complementary metal-oxide-semiconductor process
bps	Bits per second
Line contention	At least two drivers on the same bus inadvertently enabled simultaneously
LVDS	Low-voltage differential signaling
Multidrop	Multiple receivers driven by a single driver per bus line
Multipoint	Multiple transceivers, drivers, or receivers per bus line
U.L.	Unit load

Acknowledgment

Technical assistance was provided by Kevin Gingerich and Frank Dehmelt, both of the TI Advanced Analog Products Group.

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1. *Electrical Characteristics of Balanced Voltage Digital Interface Circuits,* ANSI/TIA/EIA-422-B-1994, Telecommunications Industry Association, 1994
2. *Electrical Characteristics of Generators and Receivers for Use in Balanced Digital Multipoint Systems*, ANSI/TIA/EIA-485-A-1998, Telecommunications Industry Association, 1998
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5. *Comparing EIA-485 and EIA-422-A Line Drivers and Receivers in Multipoint Applications*, John Goldie, National Semiconductor, Application Note AN-759
6. *Data Transmission Design Seminar Reference Manual*, 1998, Texas Instruments, literature number SLLE01
7. *Data Transmission Line Circuits Data Book,* 1998, Texas Instruments, literature number SLLD001

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