This document outlines additional communications formats that can be supported along with the NMRA DCC General Packet Format. These communications formats can be as simple as extra preamble bits, or another packet format in its entirety.

A. Restricted Speed Instructions (Signal-Controlled)

Restricted Speed Instructions are used to modify the speed of a train in limited track sections, based on the state of a signal. All decoders, regardless of their address, must accept and act on this information. This method of communications satisfies the following requirements:

- For safe operation, these commands must be sent as frequently as possible.
- Full control over all decoder functions must be maintained at all times.
- An operator must be able to override the Restricted Speed Instruction.
- Acceleration and Deceleration of each locomotive must be adjustable on an individual basis.
- Bridging gaps between adjacent track sections must not cause short circuits or undefined operation.

Basic Format

The basic format involves introducing additional bits between the Packet End Bit, and the start of the next Preamble. These bits are added by the Command Station, and look like extra preamble bits to most decoders in a system. Each track section on a layout where restricted speed information should be applied is connected to a 'Track Section Module'.
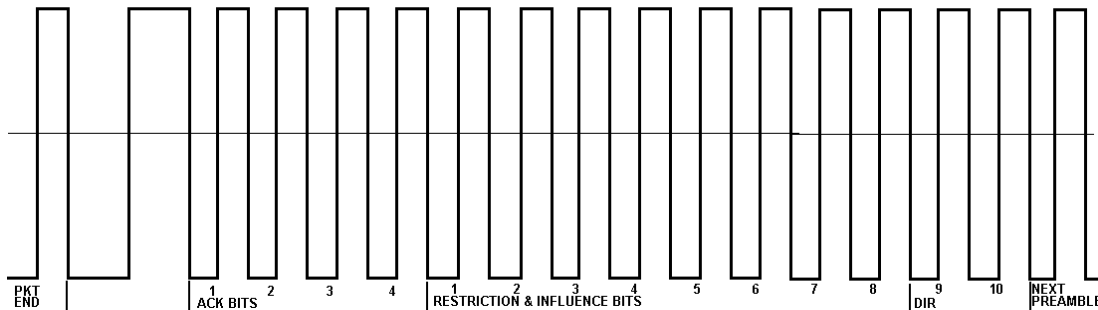
Figure 1: Output from a Command Station

The first bit after the Packet End Bit of a normal DCC packet is a zero bit, to improve error recovery. The next four one bits are ACK bits, which are used to detect locomotive feedback in a track section module. The next 10 one bits are used to restrict the speed *or* influence the function outputs of the decoder. These one bits are followed by the normal preamble for the next DCC packet. If a restricted speed is required in a particular area, the Track Section Module for that area cuts out particular bits by disconnecting power , based on the degree of restriction required.

Restricted Speed Format

The 10 Restriction & Influence bits affect the decoder's speed according to the following table:

Restriction Bit 1 is cut out	Restrict speed to 5/6 of Full Speed
Restriction Bits 1 & 2 are cut out	Restrict speed to 2/3 of Full Speed

Restriction Bits 1-3 are cut out	Restrict speed to 1/2 of Full Speed
Restriction Bits 1-4 are cut out	Restrict speed to 1/3 of Full Speed
Restriction Bits 1-5 are cut out	Restrict speed to 1/6 of Full Speed
Restriction Bits 1-7 are cut out	Stop with Normal Deceleration rate
Restriction Bits 1-8 are cut out	Emergency Stop

When the 9th bit is cut out, the restricted speed is applied in the forward/eastbound direction. If the 10th bit is cut out, the restricted speed applies in the reverse/westbound direction.
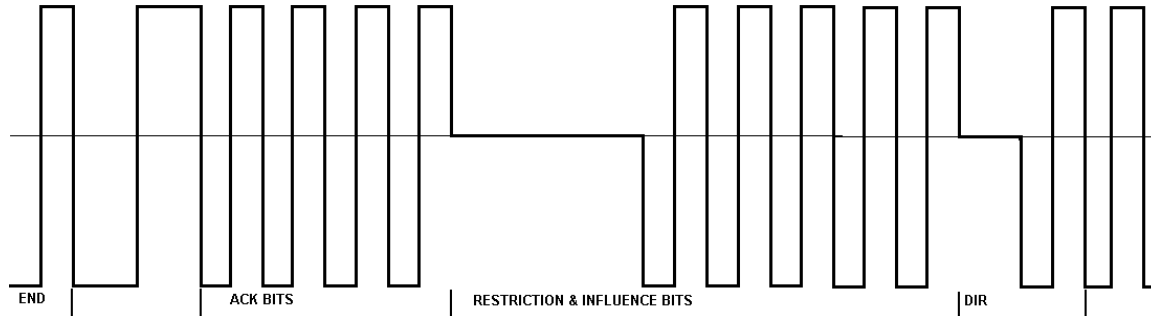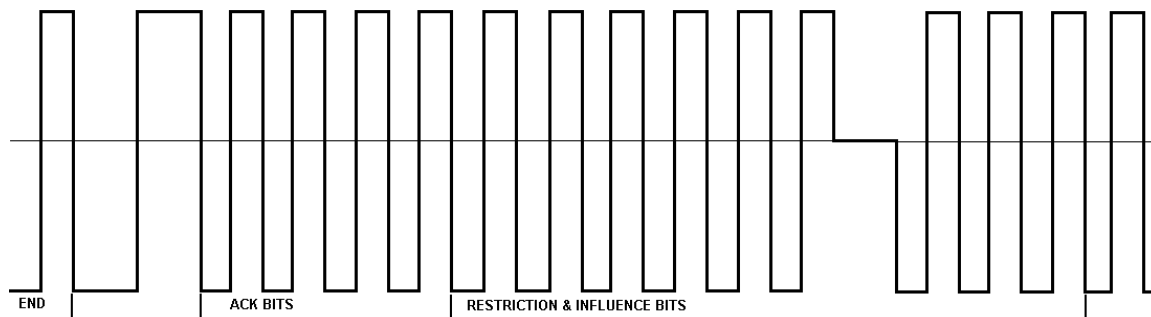

Figure 2: Half Speed Restriction from a Track Section Module

Function Influence Format

The last 8 Restriction & Influence bits are logically OR'd with the normal internal function bits according to the following table:

Influence Bit 3 is cut out	Function 1 is activated
Influence Bit 4 is cut out	Function 2 is activated
Influence Bit 5 is cut out	Function 3 is activated
Influence Bit 6 is cut out	Function 4 is activated
Influence Bit 7 is cut out	Function 5 is activated
Influence Bit 8 is cut out	Function 6 is activated
Influence Bit 9 is cut out	Function 7 is activated
Influence Bit 10 is cut out	Function 8 is activated

Figure 3: Function 5 Influenced