1394-based Digital Camera Specification

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Sponsored by:
Camera Working Group of the 1394 Trade Association

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Abstract: The purpose of this document is to act as a design guide for digital camera makers that wish to use IEEE 1394-1995 as the camera-to-PC interconnect. Adherence to the design specifications contained herein do not guarantee, but will promote interoperability for this class of device. The camera registers, fields within those registers, video formats, modes of operation, and controls for each are specified. Area has been left for growth. To make application for additional specification, contact the 1394 Trade Association Camera Working Group.

Keywords: Camera, 1394, Digital Video

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1. Digital camera control command register

Base address for all digital camera command registers is:

Bus_ID, Node_ID , FFFFFxxxxxxx (initial units space)

This address is contained in the configuration ROM in the camera unit directory.
The following sections define all the camera CSR registers. The offset field in each of the tables is the byte offset from the above base address.

1.1 Camera initialize register

Offset	Name	Field	Bit	Description
000h	INITIALIZE	Initialize	[0]	If assert this bit, Camera will re-set to initial (factory setting value) state.
		-	[1..31]	Reserved (All zero)

0-7	8-15	16-23	24-31
i	reserved (all 0)		

Initial values	Zeros
Read values	Zeros
Write effect	if '0' no effect, if '1' set initial state(Factory setting)

1.2 Inquiry register for video format/mode/frame rate

Each bit in the inquiry fields specify the availability of a given feature. A value of 1 indicates that the corresponding feature is implemented, a value of 0 indicates that the corresponding feature is not implemented.
The following sections define the inquiry registers.

1.2.1 Inquiry register for video format

Offset	Name	Field	Bit	Description
100h	V_FORMAT_INQ	Format_0	[0]	VGA non compressed format. (Maximum 640x480)
		Format_x	[1..7]	Reserved for other format.
		-	[8..31]	Reserved. (All zero)

0-7	8-15	16-23	24-31
format	reserved (all 0)		

Initial values	System dependent.
Read values	System dependent. Same value to Initial value.
Write effect	Ignored.

1.2.1.1 Inquiry register for video mode

Offset	Name	Field	Bit	Description
180h	V_MODE_INQ_0 (Format_0)	Mode_0	[0]	160 X 120 YUV(4:4:4) Mode (24bit/pixel)
		Mode_1	[1]	320 X 240 YUV(4:2:2) Mode (16bit/pixel)
		Mode_2	[2]	640 X 480 YUV(4:1:1) Mode (12bit/pixel)
		Mode_3	[3]	640 X 480 YUV(4:2:2) Mode (16bit/pixel)
		Mode_4	[4]	640 X 480 RGB Mode (24bit/pixel)
		Mode_5	[5]	640 X 480 Y (Mono) Mode (8bit/pixel)
		Mode_x	[6..7]	Reserved for another Mode
		-	[8..31]	Reserved. (All zero)
184h: 19Fh	Reserved for other V_MODE_INQ_x for Format_x.			

0-7	8-15	16-23	24-31
v_mode_inq	reserved (all 0)		

Initial values	System dependent
Read values	System dependent. Same value to Initial value
Write effect	Ignored

1.2.2 Inquiry register for video frame rate

Offset	Name	Field	Bit	Description
200h	V_RATE_INQ_0_0 (Format_0,Mode_0)	FrameRate_0	[0]	Reserved
		FrameRate_1	[1]	Reserved
		FrameRate_2	[2]	7.5fps
		FrameRate_3	[3]	15fps
		FrameRate_4	[4]	30fps
		FrameRate_x	[5..7]	Reserved for another FrameRate
		-	[8..31]	Reserved (All zero)
204h	V_RATE_INQ_0_1 (Format_0,Mode_1)	FrameRate_0	[0]	Reserved
		FrameRate_1	[1]	3.75fps
		FrameRate_2	[2]	7.5fps
		FrameRate_3	[3]	15fps
		FrameRate_4	[4]	30fps
		FrameRate_x	[5..7]	Reserved for another FrameRate
		-	[8..31]	Reserved (All zero)
208h	V_RATE_INQ_0_2 (Format_0,Mode_2)	FrameRate_0	[0]	Reserved
		FrameRate_1	[1]	3.75fps
		FrameRate_2	[2]	7.5fps
		FrameRate_3	[3]	15fps
		FrameRate_4	[4]	30fps
		FrameRate_x	[5..7]	Reserved for another FrameRate
		-	[8..31]	Reserved (All zero)
20Ch	V_RATE_INQ_0_3 (Format_0,Mode_3)	FrameRate_0	[0]	Reserved
		FrameRate_1	[1]	3.75fps
		FrameRate_2	[2]	7.5fps
		FrameRate_3	[3]	15fps
		FrameRate_4	[4]	30fps
		FrameRate_x	[5..7]	Reserved for another FrameRate
		-	[8..31]	Reserved (All zero)
210h	V_RATE_INQ_0_4 (Format_0,Mode_4)	FrameRate_0	[0]	Reserved
		FrameRate_1	[1]	3.75fps
		FrameRate_2	[2]	7.5fps
		FrameRate_3	[3]	15fps
		FrameRate_4	[4]	30fps
		FrameRate_x	[5..7]	Reserved for another FrameRate
		-	[8..31]	Reserved (All zero)
214h	V_RATE_INQ_0_5 (Format_0,Mode_5)	FrameRate_0	[0]	Reserved
		FrameRate_1	[1]	3.75fps
		FrameRate_2	[2]	7.5fps
		FrameRate_3	[3]	15fps
		FrameRate_4	[4]	30fps
		FrameRate_5	[5]	60fps
		FrameRate_x	[6..7]	Reserved for another FrameRate
		-	[8..31]	Reserved (All zero)
218h : 21F16	reserved V_RATE_INQ_0_x (for other Mode_x of Format_0)			
220h : 3FFh	reserved V_RATE_INQ_y_x (for other Format_y,Mode_x)			

0-7	8-15	16-23	24-31
frame_rate	reserved (all 0)		

Initial values	System dependent
Read values	System dependent (Same as initial value)
Write effect	Ignored

1.3 Inquiry register for basic function

All the field except "Memory_Channel" is bit assignment for inquiry.
(0:Not available 1:Available)

Offset	Name	Field	Bit	Description
400h	BASIC_FUNC_INQ		[0..15]	Reserved
		Cam_Power_Cntl	[16]	Camera process power ON/OFF capability
			[17..18]	Reserved
		One_Shot_Inq	[19]	One shot transmission capability
			[20..27]	Reserved
		Memory_Channel	[28..31]	Maximum memory channel number (N) Memory channel no 0 = Factory setting memory 1 = Memory Ch 1 2 = Memory Ch 2 : N= Memory Ch N If 0000, user memory is not available.

0-7	8-15	16-23				24-31	
		c		o			mem

Initial values	System dependent
Read values	System dependent (Same as initial value)
Write effect	Ignored

1.4 Inquiry register for feature presence

All the field is bit assignment for inquiry. (0:Not available 1:Available)

Offset	Name	Field	Bit	Description
404h	Feature_Hi_Inq	Brightness	[0]	Brightness Control
		Exposure	[1]	Exposure Control
		Sharpness	[2]	Sharpness Control
		White_Balance	[3]	White Balance Control
		Hue	[4]	Hue Control
		Saturation	[5]	Saturation Control
		Gamma	[6]	Gamma Control Or ON/OFF
		Shutter	[7]	Shutter Speed Control
		Gain	[8]	Gain Control
		Iris	[9]	IRIS Control
		Focus	[10]	Focus Control
			[11..31]	Reserved
408h	Feature_Lo_Inq	Zoom	[0]	Zoom Control
		Pan	[1]	PAN Control
		Tilt	[2]	TILT Control
			[3..31]	Reserved

offset	0-7	8-15	16-23	24-31
404h	b e s w h s g s g l f	Reserved (all zero)		
408h	z p t	Reserved (all zero)		

Initial values	System dependent
Read values	System dependent (Same as initial value)
Write effect	Ignored

1.5 Inquiry register for feature elements

All the field named xxx_Inq is bit assignment for inquiry. (0:Not available 1:Available)

Offset	Name	Field	Bit	Description
500h	BRIGHTNESS_INQ	Presence_Inq	[0]	Presence of this feature
			[1..3]	Reserved
		ReadOut_Inq	[4]	Capability of reading the value of this feature
		On/Off_Inq	[5]	Capability of switching this feature ON and OFF
		Auto_Inq	[6]	Automode (Controlled automatically by camera)
		Manual_Inq	[7]	Manual mode (Controlled by user)
		MIN_Value	[8..19]	MIN value for this feature control
		MAX_Value	[20..31]	MAX value for this feature control
504h	EXPOSURE_INQ	Same definition to BRIGHTNESS_INQ		
508h	SHARPNESS_INQ	Same definition to BRIGHTNESS_INQ		
50Ch	WHITE_BAL_INQ	Same definition to BRIGHTNESS_INQ		
510h	HUE_INQ	Same definition to BRIGHTNESS_INQ		
514h	SATURATION_INQ	Same definition to BRIGHTNESS_INQ		
518h	GAMMA_INQ	Same definition to BRIGHTNESS_INQ		
51Ch	SHUTTER_INQ	Same definition to BRIGHTNESS_INQ		
520h	GAIN_INQ	Same definition to BRIGHTNESS_INQ		
524h	IRIS_INQ	Same definition to BRIGHTNESS_INQ		
528h	FOCUS_INQ	Same definition to BRIGHTNESS_INQ		
52Ch : 57Ch	Reserved for other FEATURE_HI_INQ			
580h	ZOOM_INQ	Presence_Inq	[0]	Presence of this feature
			[1..3]	Reserved
		ReadOut_Inq	[4]	Capability of reading the value of this feature
		On/Off_Inq	[5]	Capability of switching this feature ON and OFF
		Auto_Inq	[6]	Auto mode (Controlled automatically by camera)
		Manual_Inq	[7]	Manual mode (Controlled by user)
		MIN_Value	[8..19]	MIN Value for this feature control
		MAX_Value	[20..31]	MAX Value for this feature control
584h	PAN_INQ	Same definition to ZOOM_INQ		
588h	TILT_INQ	Same definition to ZOOM_INQ		
58Ch : 5FCh	received for other FEATURE_LO_INQ			

offset	0-7	8-15	16-23	24-31
580h	p r o a m	min_value	max_value	

Initial values	System dependent
Read values	System dependent (Same as initial value)
Write effect	Ignored

1.6 Status and control registers for camera

Offset	Name	Bit	Description
600h	Cur_V_Frm_Rate	[0..2]	Current frame rate FrameRate_0 .. FrameRate_7
604h	Cur_V_Mode	[0..2]	Current video mode Mode_0 .. Mode_7
608h	Cur_V_Format	[0..2]	Current video format Format_0 .. Format_7
60Ch	ISO_Channel	[0..3]	Isochronous channel number for video data transmission
		[4..5]	Reserved
	ISO_Speed	[6..7]	Isochronous transmit speed code.
610h	Camera_Power	[0]	1 = power-up camera 0 = power-down camera.
614h	ISO_EN	[0]	1 = start ISO transmission of video data 0 = stop ISO transmission of video data
618h	Memory_Save	[0]	1 = current status and modes are saved to Mem_Save_Ch (Self Cleared)
61Ch	One_Shot	[0]	1 = only one frame of video data is transmitted (Self cleared after transmission) Ignored if ISO_EN = 1
620h	Mem_Save_Ch	[0..3]	Write channel for Memory_Save command Must be >= 0001 (0 is factory settings, which cannot be overwritten) (see BASIC_FUNC_INQ)
624h	Cur_Mem_Ch	[0..3]	When read from, returns Current Memory Channel number When written to, loads status, modes, and values from the specified memory channel

Initial values	System dependent.
Read values	Last update (Reserved bits are always zero)
Write effect	As indicated in table above

1.7 Status and control register for feature

Offset	Name	Field	Bit	Description
800h	BRIGHTNESS	Presence_Inq	[0]	Presence of this feature 0:N/A 1:Available
			[1-5]	Reserved
		ON_OFF	[6]	Write: ON or OFF this feature, Read: read a status 0: OFF, 1: ON
		A_M_Mode	[7]	Write: set the mode, Read: read a current mode 0: Manual, 1: Auto.
			[8-19]	Reserved.
		Value	[20-31]	Value. Write the value in Auto mode, this field is ignored. If "ReadOut" capability is not available, read value has no meaning
804h	EXPOSURE	Same definition to BRIGHTNESS		
808h	SHARPNESS	Same definition to BRIGHTNESS		
80Ch	WHITE_BALANCE	Presence_Inq	[0]	Presence of this feature. 0:N/A 1:Available
			[1-5]	Reserved.
		ON_OFF	[6]	Write: ON or OFF this feature, Read: read a status 0: OFF, 1: ON
		A_M_Mode	[7]	Write: set the mode, Read: read a current mode 0: Manual, 1: Auto.
		U_Value	[8-19]	U Value. Write the value in AUTO mode, this field is ignored. If "ReadOut" capability is not available, read value has no mean
		V_Value	[19-31]	V Value Write the value in AUTO mode, this field is ignored. If "ReadOut" capability is not available, read value has no mean
810h	HUE	Same definition to BRIGHTNESS		
814h	SATURATION	Same definition to BRIGHTNESS		
818h	GAMMA	Same definition to BRIGHTNESS		
81Ch	SHUTTER	Same definition to BRIGHTNESS		
820h	GAIN	Same definition to BRIGHTNESS		
824h	IRIS	Same definition to BRIGHTNESS		
828h	FOCUS	Same definition to BRIGHTNESS		
82C16 : 87C16	reserved for other FEATURE_HI			
880h	Zoom	Same definition to BRIGHTNESS		
884h	PAN	Same definition to BRIGHTNESS		
888h	TILT	Same definition to BRIGHTNESS		
88Ch : 8FCh	reserved for other FEATURE_LO			

offset	0-7				8-15	16-23	24-31
80Ch	p		o	a	reserved/u_value	value/v_value	

Initial values	System dependent
Read values	Last update values
Write effect	stored ([0] is read only)

1.8 Register map

Offset	Register
000h	<Camera initialize register> INITIALIZE
100h	<Inquiry register for video format> V_FORMAT_INQ
180h	<Inquiry register for video mode> V_MODE_INQ_x
200h	<Inquiry register for video frame rate> V_RATE_INQ_y_x
300h	
400h	<Inquiry register for feature presence> BASIC_FUNC_INQ FEATURE_HI_INQ FEATURE_LO_INQ
500h	<Inquiry register for feature elements> xxxxxxxxxx_INQ
600h	<Status and control register for camera> CAM_STA_CTRL
700h	<Reserved>
800h	<Status and control register for feature> xxxxxxxxxxx

2. Isochronous packet format

Every video format, mode and frame rate has different video data format. This version of the specification only describes VGA non compressed video format. (T.B.D. for other formats.)

2.1 Isochronous packet format for VGA non-compressed format(Format_0)

2.1.1 Video isochronous packet structure

The following table shows the format of the first quadlet in the data field of each isochronous data block.

0-7	8-15	16-23		24-31	
data_length		tg	channel	tCode	sy
header_CRC					
Video data payload					
data_CRC					

Isochronous Data Block Packet Format

Where the following fields are defined in the IEEE 1394 standard:

data_length - number of bytes in the data field

tg - tag field - shall be set to zero

channel - isochronous channel number, as programmed in the iso_channel field of the cam_sta_ctrl register

tCode - transaction code - shall be set to the isochronous data block packet tCode

sy - synchronization value - shall be set to 0001h on the first isochronous data block of a frame, and shall be set to zero on all other isochronous data blocks

Video data payload - shall contain the digital video information, as defined in the following sections

2.1.2 Video mode comparison chart

Every component Y,U,V,R,G,B has 8 bit data.

Mode	Video Format	60fps	30fps	15fps	7.5fps	3.75fps
Mode_0	160x120 YUV(4:4:4) 24bit/pixcel		1/2H 80p 60q	1/4H 40p 30q	1/8H 20p 15q	
Mode_1	320x240 YUV(4:2:2) 16bit/pixcel		1H 320p 160q	1/2H 160p 80q	1/4H 80p 40q	1/8H 40p 20q
Mode_2	640x480 YUV(4:1:1) 12bit/pixcel		2) 2H 1280p 480q	1H 640p 240q	1/2H 320p 120q	1/4H 160p 60q
Mode_3	640x480 YUV(4:2:2) 16bit/pixcel		4) 2H 1280p 640q	2) 1H 640p 320q	1/2H 320p 160q	1/4H 160p 80q
Mode_4	640x480 RGB 24bit/pixcel		4) 2H 1280p 960q	2) 1H 640p 480q	1/2H 320p 240q	1/4H 160p 120q
Mode_5	640x480 Y (Mono) 8bit/pixcel	4) 4H 2560p 640q	2) 2H 1280p 320q	1H 640p 160q	1/2H 320p 80q	1/4H 160p 40q
Mode_6	Reserved					
Mode_7	Reserved					

[---H : Line / Packet]
2) : required S200 data rate [---p : Pixel / Packet]
4) : required S400 data rate [---q : Quadlet / Packet]

2.1.3 Video data payload structure

Pn : Pixel number / packet
K : $Pn \times n$ (n = 0..N-1)
($Pn \times N$ = Total pixel number / frame.)

<YUV (4: 4: 4) format (Mode_0)>

U-(K+0)	Y-(K+0)	V-(K+0)	U-(K+1)
Y-(K+1)	V-(K+1)	U-(K+2)	Y-(K+2)
V-(K+2)	U-(K+3)	Y-(K+3)	V-(K+3)
U-(K+Pn-4)	Y-(K+Pn-4)	V-(K+Pn-4)	U-(K+Pn-3)
Y-(K+Pn-3)	V-(K+Pn-3)	U-(K+Pn-2)	Y-(K+Pn-2)
V-(K+Pn-2)	U-(K+Pn-1)	Y-(K+Pn-1)	V-(K+Pn-1)

<YUV (4: 2: 2)format (Mode_1,Mode_3)>

U-(K+0)	Y-(K+0)	V-(K+0)	Y-(K+1)
U-(K+2)	Y-(K+2)	V-(K+2)	Y-(K+3)
U-(K+4)	Y-(K+4)	V-(K+4)	Y-(K+5)
U-(K+Pn-6)	Y-(K+Pn-6)	V-(K+Pn-6)	Y-(K+Pn-5)
U-(K+Pn-4)	Y-(K+Pn-4)	V-(K+Pn-4)	Y-(K+Pn-3)
U-(K+Pn-2)	Y-(K+Pn-2)	V-(K+Pn-2)	Y-(K+Pn-1)

<YUV (4: 1: 1)format (Mode_2)>

U-(K+0)	Y-(K+0)	Y-(K+1)	V-(K+0)
Y-(K+2)	Y-(K+3)	U-(K+4)	Y-(K+4)
Y-(K+5)	V-(K+4)	Y-(K+6)	Y-(K+7)
U-(K+Pn-8)	Y-(K+Pn-8)	Y-(K+Pn-7)	V-(K+Pn-8)
Y-(K+Pn-6)	Y-(K+Pn-5)	U-(K+Pn-4)	Y-(K+Pn-4)
Y-(K+Pn-3)	V-(K+Pn-4)	Y-(K+Pn-2)	Y-(K+Pn-1)

<RGB format (Mode_4)>

R-(K+0)	G-(K+0)	B-(K+0)	R-(K+1)
G-(K+1)	B-(K+1)	R-(K+2)	G-(K+2)
B-(K+2)	R-(K+3)	G-(K+3)	B-(K+3)
R-(K+Pn-4)	G-(K+Pn-4)	B-(K+Pn-4)	R-(K+Pn-3)
G-(K+Pn-3)	B-(K+Pn-3)	R-(K+Pn-2)	G-(K+Pn-2)
B-(K+Pn-2)	R-(K+Pn-1)	G-(K+Pn-1)	B-(K+Pn-1)

<Y (Mono)format (Mode_5)>

Y-(K+0)	Y-(K+1)	Y-(K+2)	Y-(K+3)
Y-(K+4)	Y-(K+5)	Y-(K+6)	Y-(K+7)
Y-(K+Pn-8)	Y-(K+Pn-7)	Y-(K+Pn-6)	Y-(K+Pn-5)
Y-(K+Pn-4)	Y-(K+Pn-3)	Y-(K+Pn-2)	Y-(K+Pn-1)

2.1.4 Data structure

<Y, R, G, B>

Each component has 8bit data. Data type is 'Unsigned Char".

	Signal level (Decimal)	Data (Hexadecimal)
Highest	255	0xFF
	254	0xFE
	:	:
	1	0x01
Lowest	0	0x00

<U, V>

Each component has 8bit data. Data type is "Straight Binary".

	Signal level (Decimal)	Data (Hexadecimal)
Highest(+)	127	0xFF
	126	0xFE
	:	:
	1	0x81
Lowest	0	0x80
	-1	0x7F
	:	:
	-127	0x01
Highest(-)	-128	0x00

3. Serial bus management

This chapter describes the camera behavior on a given Serial Bus . (IEEE 1394 Digital Camera is in accordance with IEEE standard 1212-1991.)

3.1 Bus Management

An IEEE 1394 Digital Camera complying with this standard is a peripheral for a personal computer or workstation. Another node on the IEEE 1394 bus, such as a computer, acts as the camera controller. In order for the camera to perform any action, the camera controller must access the camera control registers, as described in this standard. A camera which is compliant with this protocol standard is a passive device. It initiates no actions of its own.

The camera is neither isochronous manager capable nor full bus manager capable. The camera is also not cycle master capable. The contents of the self_ID packet generated by the camera, and the contents of camera configuration ROM shall accurately reflect this level of capability.
In order for the camera to perform any action, it must be connected to other IEEE 1394 nodes. At a minimum, there must be a cycle master capable node and an isochronous manager capable node. In addition, there must be some node which is running application software that implements the protocol described in this standard. Note that all of these capabilities could reside in a single node.

The camera controller is responsible for the following activities related to camera operation:

1) Force a cycle master capable node to be the root

2) Start cycle master operation

3) Initialize the camera control registers for a desired video mode, frame rate, etc.

4) Allocate isochronous resources needed by the camera (isochronous channel number and bandwidth, as needed for the selected video mode)

5) Program the isochronous channel number and transmit speed into the camera control registers

6) Instruct the camera to start sourcing isochronous video data

The camera continues sourcing isochronous video data until the camera controller instructs the camera to stop. If a bus reset occurs during camera operation, the camera continues sourcing isochronous data immediately after the bus reset.

3.2 Asynchronous Transfer Capabilities

The IEEE 1394 Digital Camera shall be capable of sending and receive the asynchronous packets with a payload of up to 32 quadlets. This protocol does not use any asynchronous transactions which exceed this limit.

If a node sends a request packet to the digital camera between the request and corresponding response subaction, the digital camera will acknowledge that packet with a “busy” acknowledge code.

3.3 Isochronous Transfer Capabilities

IEEE 1394 Digital Camera is capable of being an isochronous talker. The camera is not capable of listening to a channel of isochronous data.

The digital camera is capable of transmitting isochronous data on channels 0 to 15 only, inclusive.

3.4 IEEE 1394 Specific Address Space

A IEEE 1394 camera which is compliant with this standard shall be compliant with the IEEE 1394 and IEEE 1212 standards.

The following sections define all CSR and ROM locations that the camera shall implement. All information in these sections is intended to comply with the IEEE 1394 standard. Where discrepancies arise, the IEEE 1394 standard shall prevail.
All address offset locations in these sections are with respect to a base address of:

FFFF F000 0000h

3.4.1 Implemented CSR's

The digital camera implements the following core CSR's, as required by the IEEE 1394 standard:

Offset	0-7	8-15	16-23	24-31
0000h	STATE_CLEAR			
0004h	STATE_SET			
0008h	NODE_IDS			
000Ch	RESET_START			
0010h				
0014h				
0018h	SPLIT_TIMEOUT_HI			
001Ch	SPLIT_TIMEOUT_LO			

Core CSR's

The digital camera implements the following IEEE 1394 Serial Bus dependent CSR's:

Offset	0-7	8-15	16-23	24-31
0200h	CYCLE_TIME			
0204h				
0208h				
020Ch				
0210h	BUSY_TIMEOUT			

Serial Bus Dependent CSR's

3.4.2 Configuration ROM

IEEE 1394 Digital Camera implements the Configuration ROM as defined in IEEE standard 1212-1991.

	Offset	0-7	8-15	16-23	24-31
Bus Info Block	400h	04h	crc_length	rom_crc_value	
	404h	31h	33h	39h	34h
	408h	0 0 1 0 rsv	FFh	max_rec	rsv
	40Ch	node_vendor_id			chip_id_hi
	410h	chip_id_lo			
Root Directory	414h	0004h		CRC	
	418h	03h	module_vendor_ID		
	41Ch	0Ch	rsv	1 0 0 0 0 0 1 1 1 1 0 0 0 0 0 0	
	420h	8Dh	indirect_offset		
	424h	D1h	unit_directory offset		

Root Directory

	Offset	0-7	8-15	16-23	24-31
Node unique ID leaf	0000h	0002h		CRC	
	0004h	node_vendor_id			chip_id_hi
	0008h	chip_id_lo			

Node Unique ID leaf

	Offset	0-7	8-15	16-23	24-31
Unit Directory	0000h	0003h		CRC	
	0004h	12h	unit_spec_ID (=0x00A02D)		
	0008h	13h	unit_sw_version (=0x000100)		
	000Ch	D4h	unit_dependent_directory offset		

Unit directory

	Offset	0-7	8-15	16-23	24-31
Unit Dependent Info	0000h	unit_dep_info_length		CRC	
	0004h	40h	command_regs_base		
	0008h	81h	vendor_name_leaf		
	000Ch	82h	model_name_leaf		

Unit Dependent Directory

Where:

command_regs_base is the quadlet offset from the base address of initial register space of the base address of the command registers defined in section 1 of this standard

vendor_name_leaf specifies the number of quadlets from the address of the vendor_name_leaf entry to the address of the vendor_name leaf containing an ASCII representation of the vendor name of this node

model_name_leaf specifies the number of quadlets from the address of the model_name_leaf entry to the address of the model_name leaf containing an ASCII representation of the model name of this node

3.4.3 Format of Vendor Name and Model Name Leaves

The unit dependent directory may contain pointers to information leaves which contain the ASCII name of the vendor and model name for this node. The format of these leaves is shown in the following table:

	Offset	0-7	8-15	16-23	24-31
Name Leaf	0000h	leaf_length		CRC	
	0004h	00h	00 0000h		
	0008h	0000 0000h			
	000Ch	char_0	char_1	char_2	char_3
	0010h	char_4	char_5	char_6	char_7
	0014h	char_8	...		
	n+6h	...			char_n-3
	n+Ah	char_n-2	char_n-1	NUL	NUL

Vendor Name/Model Name Leaves