"CAUTION" TO PREVENT DAMAGE TO THE DEVICE, CMOS HANDLING INSTRUCTIONS SHOULD BE FOLLOWED WHILE INSTALLING THE EPROM IN THE INTACS PROGRAMMER DEVICE.

Also the "camera" and "monitor" keys should be replaced with the camera and monitor symbol keys respectively supplied in LDH 8802. For further information refer to the "Installation Instruction" of the LDH 8802.

The product will be identified by using the type number together with the software release and version number as shown at power-up of keyboard.

5.3.3 Remote Control Line

The ROC or CMS will generate messages following the RCL protocol. An RCL message consists of 2 sync bits and 2 data bytes with a total message time of 20 msec.

The basic message is a NRZ (No Return to Zero) code wherein the data is biphase encoded. The centre of the first sync bit is used to synchronize the vertical blanking interval within the video network connected to the RCL concerned.

The CFCU converts this to an internal command and transfers it to the internal bus.

5.3.3.1 Remote Control Line format

The RS422 or V11 line uses a difference measurement between the two lines. If the difference (Va > Vb) is more than 20 mVtt (S/N = 15 dB) it generates a logic 1 and if the difference (Vb > Va) is more than 20 mVtt (S/N = 15 dB) it will become a logic 0.

The first synchronization byte is used for synchronization purposes.

The most significant bit of the second byte (B15) determines whether the message is meant for a CFC or a MSC. In all cases the LSB (B0) is sent first.

The decoding biphase data generates a logic 0 if there is a transient from 0 to 1 and a logic 1 if there is transient from 1 to 0.